APPLICATION NOTE

Application information for I²C-bus controlled TV Input Processor TDA9321 H

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Philips
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Abstract

This report gives a description of the TDA9321 H TV Input Processor, together with application aspects.

Purchase of Philips I²C components conveys a license under the I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

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Application information for I²C-bus controlled TV Input Processor TDA9321 H

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Author(s):
F. Bremer
T. Bruton
P.C.T.J. Laro
J.F.M. Luijckx

Design & Application Department, Consumer Systems Nijmegen, The Netherlands

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Summary

This report gives a description of the TDA9321 H High end Input Processor together with application aspects. The TDA9321 H is the successor of the TDA914X. It has a higher degree of integration and additional features. The TDA9321 H combines perfectly with the TDA933X H deflection / RGB output processor.

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1. INTRODUCTION

This report gives a description of the TDA9321 H high end input processor together with application aspects. The TDA9321 H is the successor of the TDA914X family. It has a higher degree of integration and additional features.

The TDA9321 H contains a QSS IF part with video and sound processing (including AM), a very versatile input switch block for CVBS and YC signals, a multistandard colour decoder with integrated baseband delay line, two RGB inputs, horizontal / vertical synchronisation and YUV / synchronisation outputs, all with I²C control. It is designed for use with PAL^{plus} processing.

As mentioned, the TDA9321 H also includes the vision-IF part. Compared to a stand alone IC's for vision-IF only the TDA9321 H has the advantage that I^{2}C bus commands are available for many control functions and alignment. Optimal performance is achieved by using timing signals which can be derived from the synchronization part.

The number of external components required for application is considerably less than equivalent two or three chip concepts. All necessary alignments can be done via I²C control.

The device is optimal for high end applications where many inputs are needed, where processing of YUV signals is needed (e.g. picture improvement, PAL^{plus} processing) or the display is running on another frequency (upconversion, 100 Hz or progressive scan).

For these applications a suitable deflection/RGB processor is available, the TDA933X H high end output processor, which matches ideal with the TDA9321 H.

The device is available in QFP 64 (Quad Flat Pack, 64 pins, SOT319-2)

The complete integration of all functions on a single chip has been realised using the BIMOS technology (combined BIpolar and MOS). The high frequent bipolar process is used for video processing like IF vision and various filters. The MOS process is used for all digital parts.
Due to MOS components, it is possible to integrate very large time constants.

2. DEVICE INFORMATION

The TDA9321 H is a high end input processor for applications, needing a flexible CVBS/YC input switch block and/or with additional YUV processing. Together with the TDA933X H high end output processor a flexible set architecture can be set up for scan conversion (100 Hz, progressive scan), PAL^{plus} decoding etc.

The TDA9321 H includes the video processing from IF to YUV out and QSS IF sound processing for high performance. A versatile CVBS/YC input switch block is included with two independent CVBS outputs, also 2 RGB inputs (or one RGB and one YUV input) are present which are converted to YUV for further processing. The colour decoder is full multi-standard including SECAM and Latin America systems and the base band delay line is integrated. The synchronisation part delivers horizontal and vertical synchronisation pulses for further processing. The IC has full I^{2}C control for all functions. Only one (I^{2}C) alignment is necessary for the IF PLL.

Below, a survey is given of the main features per functional block:

IF
- Vision IF amplifier with high sensitivity and good figures for differential phase and gain
- PLL demodulator with high linearity
- Alignment PLL via I²C
- Multistandard IF with negative and positive modulation, switchable via I^{2}C
- Switchable group delay correction circuit which can be used to compensate BG-standard in multi system sets
- Separate SIF input for single reference QSS mode and separate AGC circuit
- AM demodulator without external reference circuit
- 2 universal I^{2}C switch outputs, which can be used to switch traps, sound pass filters, etc.

Filters and Switches
- Flexible video source select with CVBS input for the internal signal, four external video inputs (two switchable for CVBS or Y/C)
- 2 three-level inputs for indication status level on pin 8 of SCART, level readout via I^{2}C
- The output signal of the video source select is externally available (also as CVBS when Y/C input is used)
- Two independent CVBS outputs for PIP, TXT, record out or other purpose (also as CVBS when Y/C input is used)
- Comb filter interface including two control lines for use with TDA4961 combfilter
- 2 linear RGB inputs with fast blanking, one switchable as YUV input, RGB is converted to YUV out
- Standard level YUV output
- Integrated luminance delay line with via I^{2}C adjustable delay
- Integrated chroma trap (auto calibrated)
- Integrated chroma bandpass filters with switchable centre frequency (auto calibrated)
- ACC and ACL control

Colour decoder
- Full multi system colour demodulator for PAL, NTSC and SECAM with option for 4 X-tals to cover all known colour standards including Latin America.
- Automatic search system for detection of colour standard
- Full PAL^{plus} helper demodulation with correct setups and levels at YUV output
- Optional blanking of “helper” signals for PAL^{plus} and EDTV-2

Synchronisation and Deflection
- Horizontal synchronisation with PLL control loop and alignment free horizontal oscillator
- Switchable time constants for ϕ1 (auto or via I^{2}C) and switchable macrovision gating
- Horizontal output choice of H_A pulse related to the synchronisation pulse or CLP pulse related to clamping pulse, also input of external clamp pulse possible
- Vertical count-down circuit for stable behaviour with provisions for non-standard signals
- Vertical output with V_A pulse for further processing

Control
- Full I²C bus control, as well for customer controls as for factory alignment
- All automatic control settings have an option for forced mode

Power consumption
- Low power consumption

Packaging
- QFP-64 (Quad Flat Pack, 64 pins SOT 319-2)

Application
- Small amount of peripheral components compared with competition IC's

2.1 Pinning configuration QFP-64 package

The TDA9321 H is available in Quad Flat Package QFP-64 SOT 319-2.

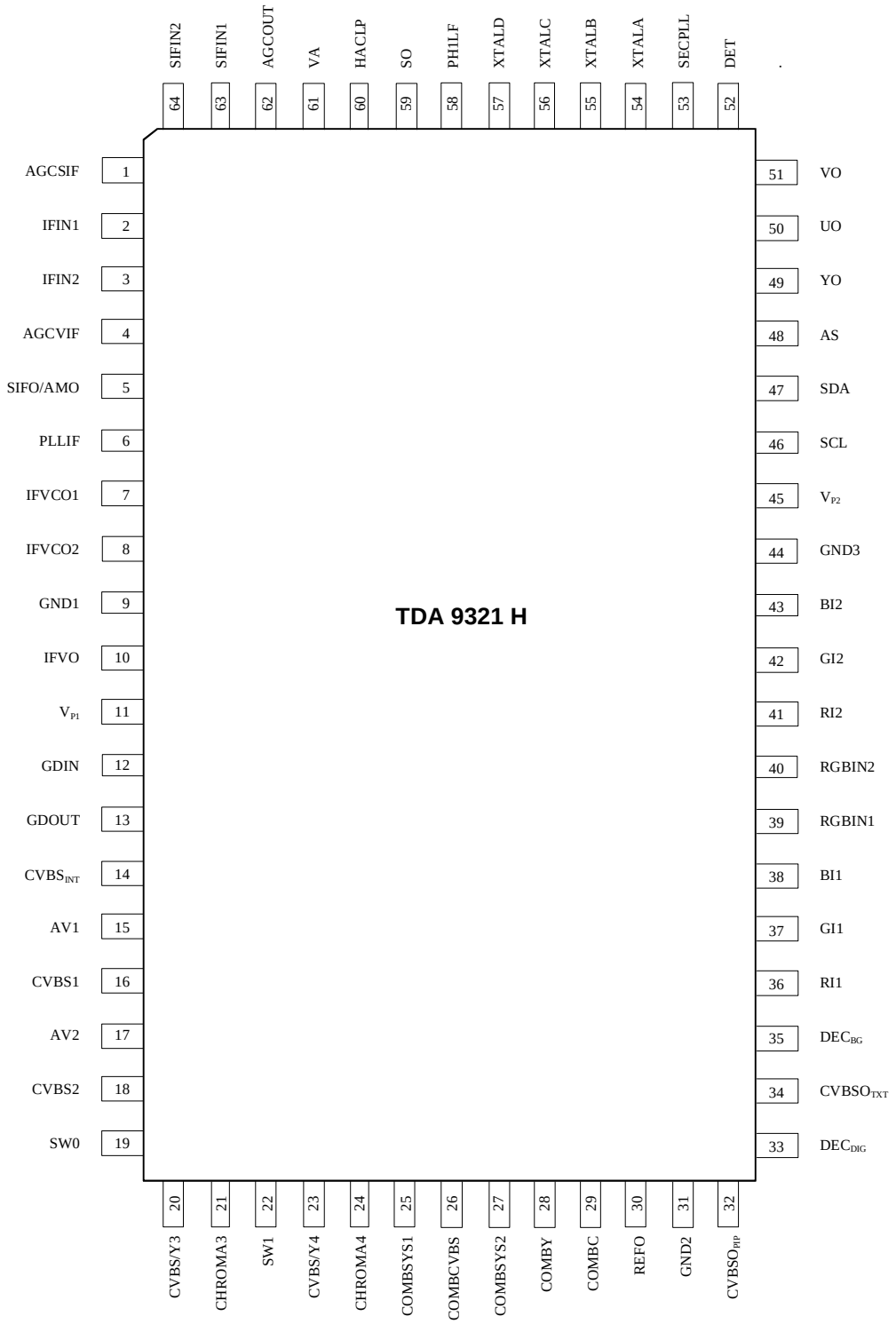


Fig 1 : Pinning diagram of QFP-64

2.2 Device description per functional block

The TDA9321 H is organised in functional blocks. These different blocks are:

Vision and sound IF
Horizontal and vertical synchronisation
Filters and Switches
Colour decoder and PAL^{plus} demodulation
Supply decoupling
Control I²C bus

A description of each functional block has been made together with the corresponding block diagrams.

In the table below, all pin numbers are given with the page number where application information can be found.

Pin	Page	**Pin**	Page	**Pin**	Page	**Pin**	Page
1	70	**17**	77	**33**	83	**49**	78
2	63	**18**	76	**34**	76	**50**	78
3	63	**19**	71	**35**	84	**51**	78
4	69	**20**	76	**36**	77	**52**	82
5	70	**21**	76	**37**	77	**53**	82
6	69	**22**	71	**38**	77	**54**	79
7	63	**23**	76	**39**	78	**55**	79
8	63	**24**	76	**40**	78	**56**	79
9	84	**25**	82	**41**	77	**57**	79
10	67	**26**	76	**42**	77	**58**	72
11	83	**27**	82	**43**	77	**59**	72
12	67	**28**	76	**44**	84	**60**	73
13	68	**29**	76	**45**	83	**61**	73
14	75	**30**	82	**46**	-	**62**	70
15	77	**31**	84	**47**	-	**63**	70
16	76	**32**	76	**48**	-	**64**	70

Table 1 : Application info per pin number

2.2.1 Vision & Sound IF

See also the related block diagram as well as the circuit diagrams at the end of the report.

The main functions are:
- -> Vision IF
  - IF amplifier plus AGC and tuner AGC control
  - PLL-demodulator and VCO
  - Video buffer
  - Groupdelay
  - Identification for: AFC, Video and PLL-LOCK
- -> Sound IF
  - IF amplifier plus AGC
  - QSS mixer and AM demodulator

These functions will be described next in this section.

The TDA9321 H includes an integrated vision-IF. Advantages compared to a stand alone IC for vision-IF only are:
- I^2C bus commands are available for many control functions and alignment. This saves pins and external components.
- Optimal performance is achieved by means of timing/gating signals derived from the synchronization part.
- Build-in accuracy of circuits is derived by use of the available chroma crystal oscillator.

*** IF-amplifier**
The IF-amplifier has symmetrical inputs and consists of three AC coupled differential gain stages with AGC function. Due to the AC coupling, biasing is simple so that cascades can be used and no DC feedback is necessary. The gain control range of the IF amplifier is 70dB minimal. The input sensitivity for AGC onset is 35 µV typical. The maximal IF-gain can be reduced with 20dB by means of I²C bus **IFS**. The high frequency range of 32-60MHz makes the amplifier suitable for multistandard application.

*** PLL-demodulator and VCO**
The IF-signal is demodulated with the help of a PLL detector. The PLL detector is used to regenerate a reference signal that is in phase to the IF-carrier signal. Demodulation is achieved by multiplying this reference signal (that is free from video contents) with the incoming IF-signal.
Switching between positive and negative modulation is done by means of I²C bus bit **MOD**.
A low pass filter after the demodulator output reduces the higher frequency demodulation products.

The voltage controlled oscillator, VCO, makes use of a reference tuned circuit that is connected externally between pins 7 and 8. The VCO is running at the double IF-frequency which prevents self locking of the PLL.
The catching range of the PLL is 2.7MHz. Within this range (and the PLL is in-lock) the performance of the demodulator is independent of the incoming IF-frequency. This automatic tracking is achieved by feedback of the PLL loopfilter voltage to internal varicaps in the VCO.

The VCO does not need an adjustable coil. The VCO frequency can be adjusted fully automatically by I²C bus in 128 steps. The resolution is 29kHz/step which gives a tuning range of 3.7MHz.
The frequency adjustment is achieved by internal switchable capacitors at the VCO input.
For SECAM L' a frequency shift can be made of typical -5.5MHz (38.9MHz -> 33.4MHz) by means of I²C bus bit **L'FA**.
For a correct demodulation, the VCO output frequency is divided by two in order to have the same frequency for both reference and IF-input signal. With the aid of the divider circuit it is also easy to achieve exactly the required 0 and 90 degrees signals.

The PLL loopfilter is connected to pin 6. In order to ensure a fast catching, an acquisition help has been provided by means of the "FPLL", Frequency Phase Lock Loop. This frequency detector gives an output signal to the PLL loopfilter as long as a difference in frequency is detected.
Due to this additional FPPL circuit the loopfilter can be fixed and does not need to be switchable.
The PLL loopfilter time constant can be made fast via Fast Filter IF-PLL, **FFI.** This function has been made available to handle RF-transmitter signals with large phase modulation (for special market areas).

*** Video buffer**
The video buffer is required to provide a low ohmic video output with the right amplitude and to protect this output for the occurrence of noise peaks, refer to figure below. The video buffer also contains a level shifter and gain stage for positive and negative modulation in order to provide a correct video amplitude and DC level.

The video buffer bandwidth is typical 9 MHz. The video output amplitude is 2.5Vpp (sync inclusive), independent of the supply voltage.
A white spot clamp prevents the video amplitude becoming greater than 6.0V typical.
A noise clamp prevents the video output becoming less than 1.5V typical. (Top sync is approx. 2V) For strong signal only, the noise peak is inverted to black level 2.7V.

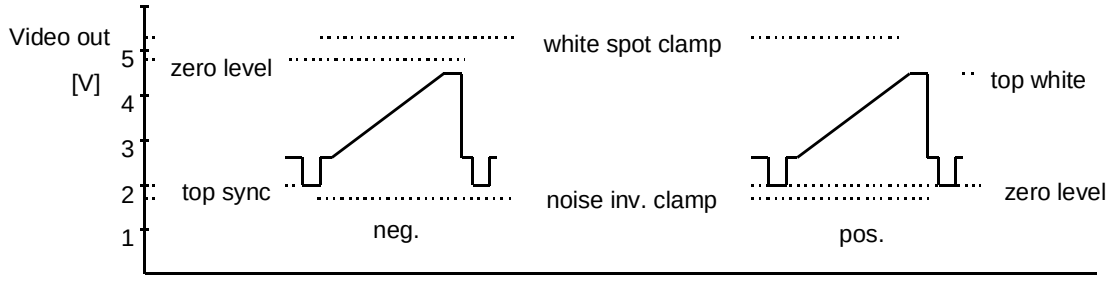


Fig 2 : Video signal for negative and positive modulation

The IF part can be switched-off by means of I²C bus command **VSW**. The internal CVBS input than can be used (with minimum components) as external input, for instance for satellite. By means of **IFO**
the IF-part can be made currentless for minimal dissipation.

*** AGC**
An AGC system controls the IF amplifier gain such that the video output amplitude is constant.
The demodulated video signal is supplied, via a low pass filter, to an AGC detector with external decoupling capacitor. The AGC detector voltage controls directly the IF gain stages.

Negative/positive modulation:
For optimal AGC behaviour the charge and discharge current of the AGC are chosen so that both, a relative fast AGC, as well a low tilt are possible for positive and negative modulated signals with the same AGC capacitor.
A SECAM-L speed-up circuit improves the AGC settling time after IF-signal loss.

With tilt is mend the video amplitude variation due to less "memory" function of the AGC capacitor). In Fig 3 the tilt is given during a field period for positive modulated signals. For negative modulated signals the tilt is line frequent.
For negative modulated signals the AGC is a top sync detector.

Positive modulation:
For positive modulated signals the AGC is a top white AGC including black level clamp which making the video amplitude independent of video contents.

A top white AGC requires a 100% white reference pulse in order to be independent of video contents. Suitable for that purpose is the white pulse (Video Insertion Test Signal, VITS) in line 17 and 330 - see Fig 3 .
Because the time constant is large (AGC current is decreased for positive modulation) the AGC will be independent of the video contents between the reference pulses.
The maximum tilt per field is defined by the external capacitor, the AGC steepness and the small discharge current in this mode.

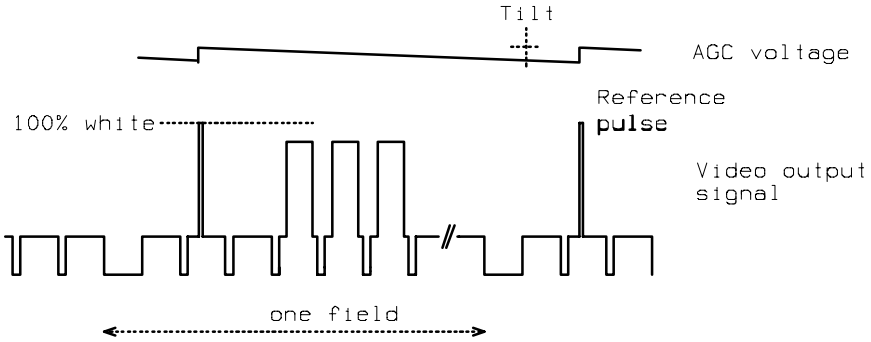


Fig 3 : Positive modulated signal with top white reference pulse

This top white AGC however is not optimal for those signals that have neither a white reference pulse or white video information (e.g. with some VCR signals). Due to the top level AGC principle a gray scene becomes white and a dark scene becomes gray, see Fig 4 . This behaviour can be avoided by means of the black level clamp.

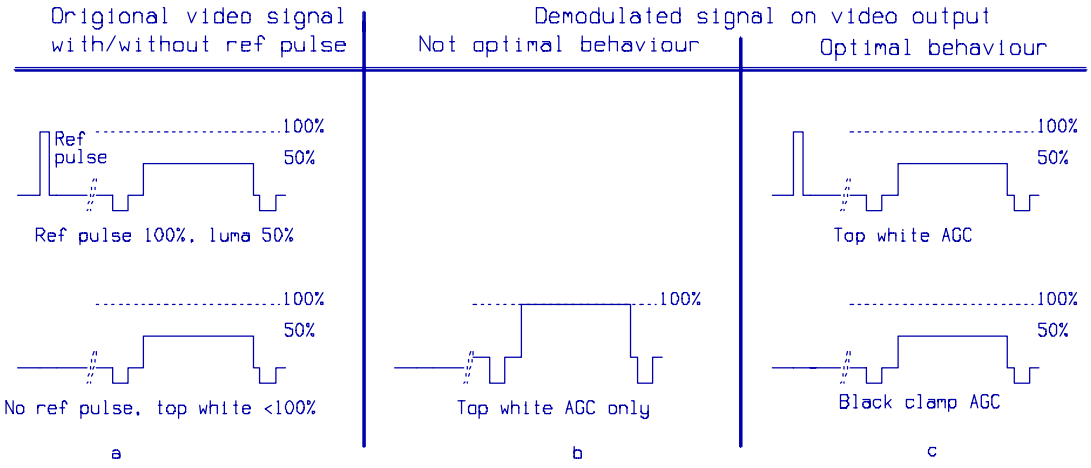


Fig 4 : Top white and black clamp AGC

The Fig 4 “b” shows that the video amplitude is increased by the top white AGC, such that 100% white is obtained. As a consequence the black level increases also.
The black level clamp AGC in “c” prevents this behaviour and becomes automatically active if the video black level on the video output increases.

In the external mode only the top white AGC is active. The black clamp AGC than is switched off because the internal signal is not synchronised any more to the horizontal oscillator.

SECAM-L speed-up circuit:
In case of positive modulation and large reduction of the incoming IF-input level a speed-up circuit is needed. This because the AGC action is slow since the AGC discharge current is small (450nA), for minimizing the tilt.
The speed-up circuit measures the amplitude of the video output signal and will react after approximately 60ms if the video output is continuously below 80% white level.
If the speed-up is activated the AGC capacitor will be discharged with a current of 50µA.

*** Tuner AGC**
The tuner AGC is provided to reduce the tuner gain and thus the tuner output voltage when receiving strong RF signals. The tuner AGC takes over when the IF input reaches a certain input level, that can be adjusted by I²C function **AGC take over**. The tuner gain can be reduced by means of the open collector output pin 62.

*** AFC**
The PLL loopfilter voltage is inverse proportional to the frequency of the incoming IF-frequency, see Fig 15. For this reason the loopfilter voltage can be used for AFC information. The "analogue AFC" voltage is amplified and fed to a window comparator. The AFC output is available by the I²C bus outputs **AFA**, **AFB.** The AFC window width can be increased by means of I²C bus **AFW**. Search tuning can be done with different frequency steps.

Due to the use of PLL detector, the AFC information is independent from video contents.
Notice that the AFC information is only valid when the PLL is in-lock, thus **PL**=1.

*** Video identification**
The IF-part includes a stand alone video identification circuit, independent of the sync part. The ident output is available by I²C bus, **IFI**, and can be used during search tuning and for automatic sound mute in full scart application. The video ident circuit measures the main frequency of the input signal which should be approximately 16kHz.
The video ident can be connected to the "internal" video signal/ or to the selected CVBS input signal. See Fig 5.

*** PLL-LOCK identification**
The TDA9321 H provides a new identification bit that indicates whether the IF-PLL is inlock. This bit can be used to optimise the search tuning algorithm.

*** Group delay**
The TDA9321 H contains a group delay correction circuit which can be switched between system BG and flat group delay response charactersistic. This has the advantage that in multi-standard receivers no compromise has to be made for the choice of the SAW filter. Both the input and output of the group delay correction circuit are externally available so that the sound trap can be connected between the IF video output and group delay correction input. The output signal of the correction circuit can be supplied to the video processing circuit and the SCART plug.

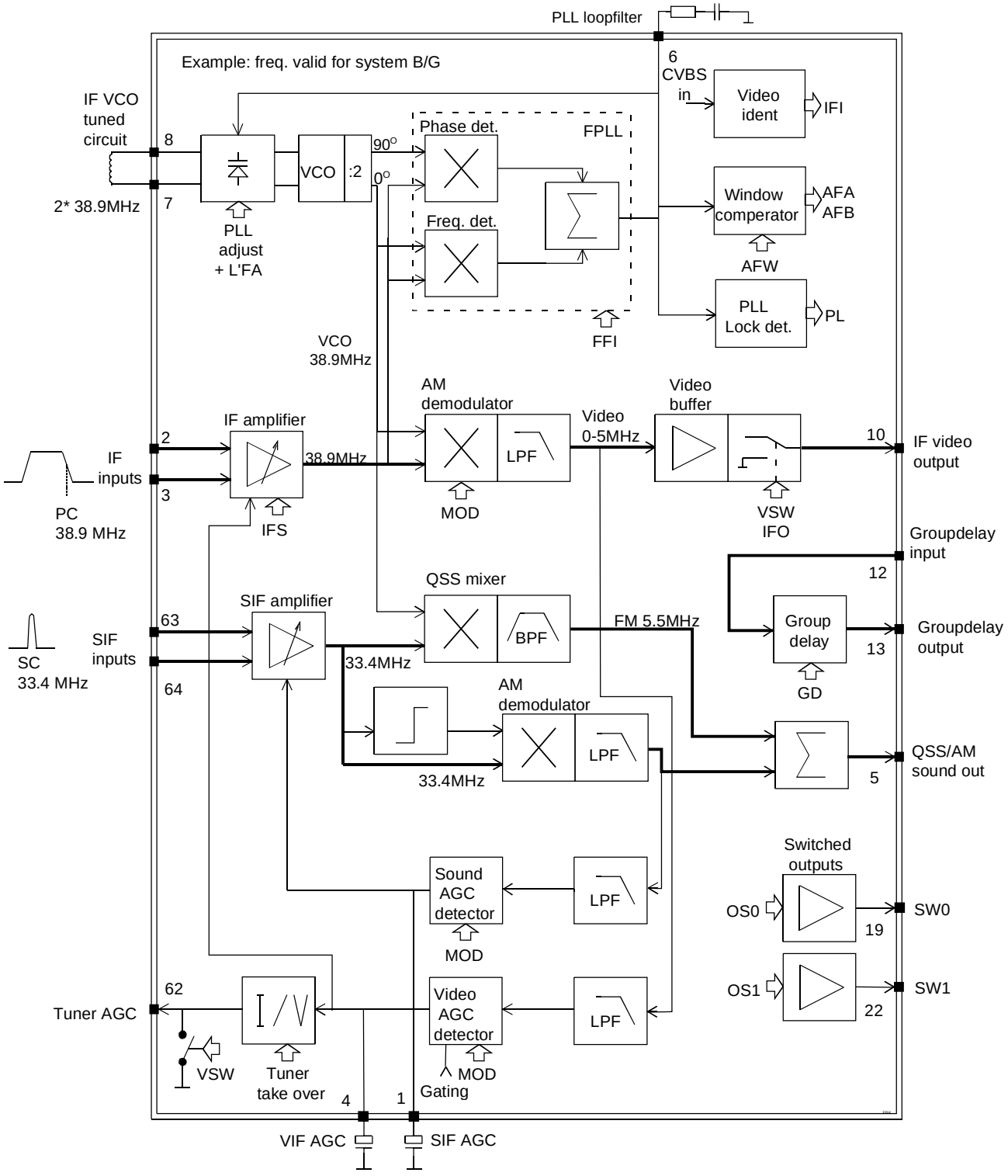
*** Sound circuit**
The TDA9321 H allows quasi split sound applications for an FM and AM output signal.
The sound IF amplifier is identical to the vision IF amplifier. The AGC is related to the SIF carrier levels (average level of AM or FM carriers) and ensures a constant signal amplitude of the AM demodulator and the QSS mixer. The AGC time constant is automatically adapted for positive and negative modulation (AGC is slow and fast respectively).

The single reference QSS mixer is realised by a multiplier. In this multiplier the SIF signal is converted to the intercarrier frequency by mixing it with the regenerated picture carrier from the VCO. The mixer output signal is supplied to the output via a high pass filter for attenuation of the residual video signals. With this system a high performance stereo sound processing can be achieved.

The AM sound demodulator is realised by a multiplier. The modulated sound IF signal is multiplied in phase with the limited SIF signal. The demodulator output is supplied to the output via a low-pass filter for attenuation of the carrier harmonics. Both QSS and AM signals are available at one output pin.

*** Switched outputs**

The TDA9321 H has two I2C bus controlled (**OS0, OS1**) output ports which can be used to switch sound traps, SAW filters or other external components.



A 1 : Block diagram: Vision & Sound IF

2.2.2 Horizontal and vertical synchronization

See also the related block diagram as well as the diagrams at the end of the report.

The main functions are:
* Horizontal sync separator
* Horizontal oscillator and calibration system
* PHI-1 detector and PLL loop
* Horizontal output
* Coincidence detector
* Noise detector
* Vertical sync separator
* Vertical divider system
* Vertical output

Before describing the functional blocks, first the various identification signals are discussed. They play an important role in the sync system behaviour and knowing their working and interrelations helps to better understand the sync system behaviour.

*** Identification signals**
The video processor includes several identification circuits. There are a number of identification signals, generated by other blocks, which influence the synchronisation behaviour. Also there are identification signals, generated by the sync block itself, which are partly used inside the sync block and/or are meant for use by other blocks. See both Fig 5 below and Fig 6.

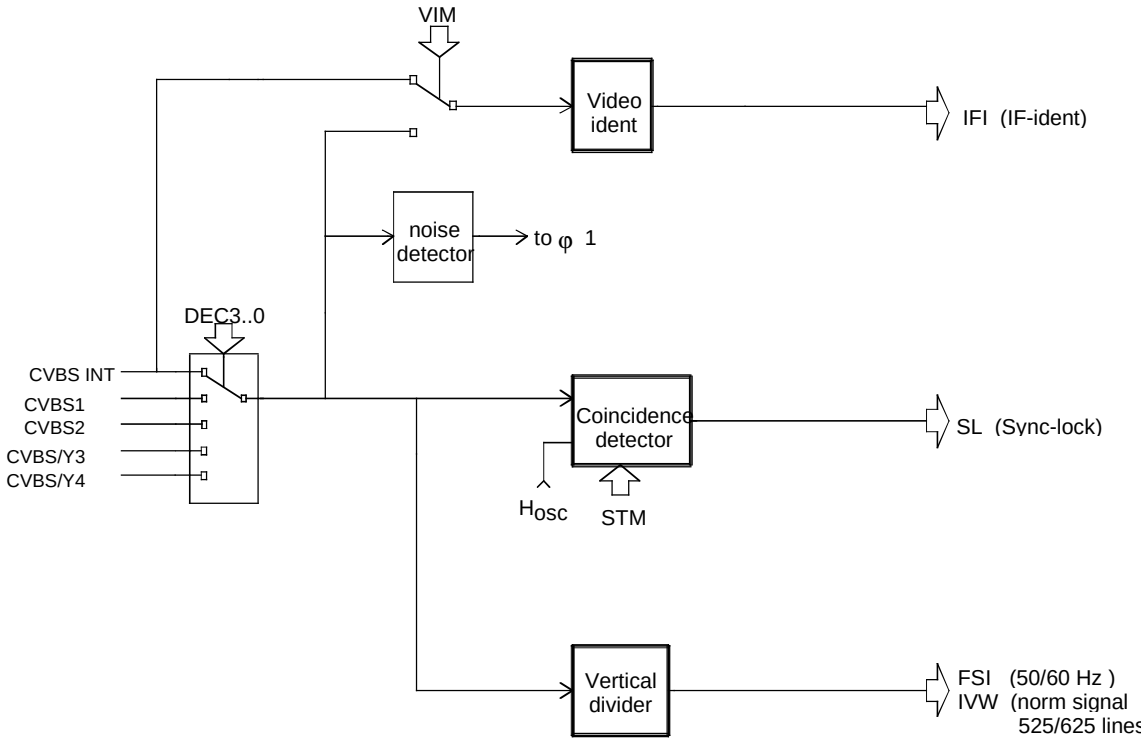


Fig 5 : Identification function

- Video ident: identifies a line frequent video signal.
  The output **IFI** (Video Ident) can be used for:
  - search tuning. For reliable transmitter detection, **IFI** should be used together with **SL** and **IVW** (see coincidence detector and vertical divider section below).
  - switching automatically the PHI-1 for stable OSD (On Screen Display) at no signal (when **VID**, video ident enable, is low)
  - switching the PHI-1 for very stable OSD/Blue Mute using **POC** (PHI-1 off, detecting signal with **IFI**)

  With **VIM** (Video ident mode) the video ident **IFI** can be connected to either the internal CVBS input (IF) pin 14 or the output of CVBS switches (selected source).

- Coincidence detector: in-lock detection of the horizontal oscillator.
  The output **SL** (Sync lock) can be used for:
  - search tuning. Also here for reliable transmitter detection, **SL** can be used together with **IVW** (see vertical divider section below).
  - out of-lock information to be displayed via OSD
  - automatic switching the PHI-1 for fast catching

  The sensitivity of **SL** can be reduced (about 5 dB) with control bit **STM** (Search Tuning Mode). This can prevent too many false stops during search tuning.

  The main difference using **SL** or **IFI**:
  - **SL** sensitivity and reliability is better than **IFI**. When IFI is used for signal identification, it is advised to check **SL** before taking important decisions like storing transmitters and muting displayed video or sound.
    Also for maximum sensitivity during search tuning, it is best to use **SL**.
  - **IFI** can be used to monitor the incoming signal from IF independent of the chosen source (useful for keeping tuned and/or muting CVBS tuner out for SCART application.). **SL** is always related to the displayed signal.
  - **IFI** is also available to detect a valid signal when the PHI-1 loop is completely switched off using **POC** (**SL** is not valid then) e.g. when a company logo is displayed at no signal condition.

- Vertical divider:
  Two output signals are available: **FSI** (50/60Hz indication) and **IVW**:
  - **FSI** gives the vertical divider mode: 50 or 60Hz, useful for correct OSD positioning on screen.
  - **IVW** becomes high when video signals are detected with a line number between 522 - 528 or 622 - 628 per frame indicating a signal near or fulfilling the TV norm. **IVW** can be used together with **IFI** or **SL** during search tuning to decide whether data is to be stored.

- Miscellaneous:
  - Noise detector: Connected to the selected video source. Used to switch the PHI-1 time constant. See separate function description.

*** Main function description**
Next, the main functions for sync will be described.

*** Horizontal sync separator**
The horizontal sync separator is supplied from the CVBS/Y inputs (chosen video source). For horizontal synchronisation the sync separator slices in the middle of the sync pulse and the slicing level is independent of the sync pulse amplitude. For the vertical synchronisation the sync pulse is sliced at a level of about 30% (closer to the black level). This ensures optimal output signals for a stable horizontal and vertical deflection under various video input conditions.
The top sync level is clamped at the CVBS input. The black level is stored internally.

*** Horizontal oscillator and calibration system**

The horizontal oscillator requires no external components and is fully integrated. The adjustment for nominal frequency is derived automatically by a calibration circuit.

The oscillator runs at a frequency of 440 Fh (440 * 15625 = 6.875 MHz). This oscillator signal is used via a divider chain to derive several other gating and timing signals.

After calibration the horizontal oscillator is controlled by the PHI-1 loop for synchronisation with the incoming video input signal.

The calibrator is responsible for the automatic adjustment of the horizontal oscillator. One of the colour crystals is being used as reference. **For that reason a correct setting by XD..XA (Xtal definition) is very important.**

Calibration occurs during the vertical retrace period and only under following conditions:

- At power-on/ initialisation (**POR** = 1)
- After power dip (shutdown detection), re-initialisation is required. (**POR** = 1)
- After loss of synchronisation (e.g. after channel switching)

Note that after power-on, the H_A/CLP output pulses are suppressed till calibration has taken place, i.e. till after **POR** becomes 0, all I^2C registers have been written and calibration was succesful.

*** PHI-1 detector**

The PHI-1 detector is a PLL circuit that synchronises the horizontal oscillator with the incoming video signal. The PLL compares the output of the H-sync separator with the horizontal oscillator. The PLL output current is converted to a voltage by means of the external loop filter. This voltage controls the horizontal oscillator.The loop filter is connected externally so the time constant can be defined according to the customer requirements. Because the static loop gain is very high there will be no phase shift when switching between input signals with different line frequencies (e.g. Fh with 50 and 60 Hz. systems). Following figure gives the functions that are effecting the PHI-1 loop time constant.

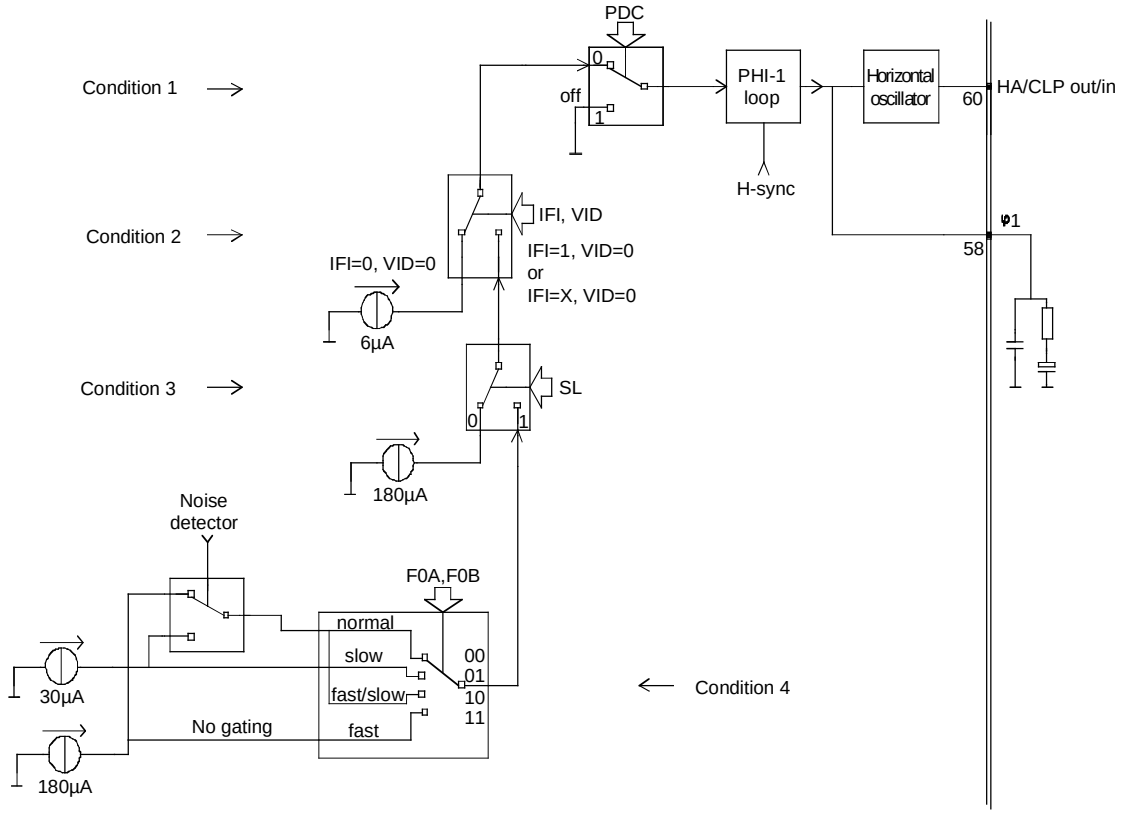


Fig 6 : PHI-1 Loop

Following conditions can be distinguished, see table below.

	Condition PHI-1 loop	Control bit via I²C	Function suitable for:
1	Completely off	**POC** set to 1 (use **IFI** or external ident circuit to detect valid incoming signal, **SL** not valid)	Very stable OSD, Blue Mute
2	Very slow	**IFI** reads 0, **VID** set to 0	Stable OSD during search
3	Out-lock	**SL** reads 0	Automatic fast settling PHI-1
4	In-lock, normal operation	**FOA/FOB**	4 time constants available for optimal for TV/VCR

Table 2 : Condition PHI-1 loop

For normal in-lock operation, condition 4, the PHI-1 time constant can be selected by **FOA/FOB**. In practice, three of the four settings are practical to use. Following table explains the three relevant **FOA/FOB** settings. Below the table, some suggestions are given how to use these functions.

FOA/FOB	PHI-1 time constant	PHI-1 gating	Suitable for:
0 0	Fast/slow (1), "auto"	yes, in slow only	Off air reception + VCR via antenna(2)(compromise) Ext.input for general use(2)(VCR, CD-I,descramblers)
1 0	Fast/slow (1)	yes	Off air reception only, high noise immunity (gating)
1 1	Fast	no	Special VCR program number ("0") External input, optimal for VCR, CD-I

Table 3 : PHI-1 time constant selection

(1) Fast or slow depends on whether the noise detector is activated.
(2) Not suitable for weak VCR signals via antenna (this due to active gating in the slow mode).

Normal off-air reception conditions or cable:
- Use **FOA/FOB** = 0 0 for program numbers. VCR reception via antenna possible on all program numbers.
- Use **FOA/FOB** = 1 1 for external input (VCR, CD-I)

Difficult off-air reception conditions (weak signal and/or interference):
- Use **FOA/FOB** = 1 0 for program numbers (optimal off-air reception due to gating)
- Use **FOA/FOB** = 1 1 for special program number (program 0) for VCR reception via antenna
- Use **FOA/FOB** = 1 1 for external input (VCR, CD-I)

***Sandcastle**
The synchronisation part generates a 2-level sandcastle pulse. Normal the output level is low, during horizontal and vertical blanking it is 2.5 V typical and during burstkey 5 V typical. See the figure below.

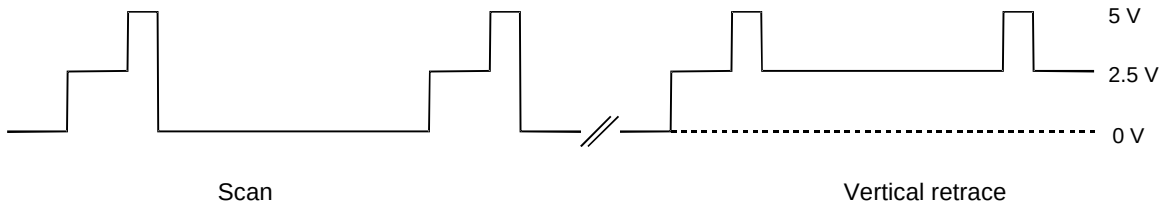


Fig 7 : Sandcastle waveform

The sandcastle can be used by external IC's for horizontal and vertical blanking, clamping synchronised signals on the backporch and keying out the burstkey of synchronised CVBS signals.

*** Horizontal input/output**
The H_A/CLP pin 60 can be used as in- or output:

Output function, internal clamp mode
This mode is selected when **ECL** = 0. Horizontal pulses are provided at pin 60 which can be used for synchronisation of further processing of the YUV outputs and synchronisation of the deflection drive for the display.
Two pulses are available, H_A and CLP, the selection is made with the bit **HO**:

- CLP pulse (**HO** = 0)
  This pulse has the same timing as the burstkey/clamping pulse on the sandcastle and has a typical width of 3.6 µs..
- H_A pulse (**HO** = 1)
  The timing of H_A is the same as the incoming sync pulse of the selected CVBS/Y signal, with some delay (0.45 µs) due to the low pass filter in the sync seperator part. The typical width is 4.7 µs.

Both pulses are positive, the low level is typical 0.2 Volt and the high level 5 Volt.
The two pulses give maximum flexibility for further processing like deflection processors (e.g. TDA 9150/51), combined RGB output/deflection processors (e.g. TDA 933X H) and scan conversion boxes like 100 Hz or progressive scan.
After power-on, the H_A/CLP output pulses are suppressed until calibration of the horizontal oscillator has taken place, see "horizontal oscillator and calibration system".

Input function, external clamp mode
This mode is meant for insertion of YUV/RGB signals, accompanied by suitable positive horizontal (clamp) and vertical timing pulses. In this way, it is not needed to feed a synchronised composite sync signal to one of the CVBS/YC inputs.
By setting **ECL** = 1, pin 60 is switched to high ohmic input and at the same time the vertical pulse V_A at output pin 61 is suppressed. In this external clamp mode it is possible to feed an external clamp pulse to pin 60. This external clamp pulse is then used internally for all clamping actions at both YUV/RGB inputs. The timing of this pulse should therefore be correct with respect to the applied YUV/RGB signals at the inputs and regarding timing preferably be comparable with the internal generated CLP pulse.
The external clamp pulse should be positive, the input can interface with all standard 5 Volt logic outputs.
In external mode, the external offered clamp pulse should also be used for further processing of the YUV outputs. So when this mode is used, it is logical to select for internal mode also the CLP pulse as output pulse. Because also the vertical V_A pulse is suppressed, an external vertical pulse should be provided if this is necessary for further processing.

*** Noise detector**

The synchronisation circuit has an internal noise detector. If the PHI-1 **FOA/FOB** is set to 0 0 (Automatic mode) or 1 0 (Gated mode) the noise detector is used to switch the time constant of the horizontal PLL. The input of the detector is connected to the selected CVBS/YC input.

The noise detector measures the RMS value of the noise during a part of the sync pulse. (The detection level is 100mVrms and corresponds to 20dB S/N-ratio for 1Vpp CVBS).

A field counter is used for hysteresis and decides after 2 successive fields whether noise is detected. When noise is detected the horizontal PLL time constant is switched to slow.

The output of the noise detector is also available via **SNR**, when the signal to noise ratio becomes less than 20 dB, **SNR** becomes 1.

*** Coincidence detector (Synchronisation Lock SL)**

The coincidence detector detects whether the incoming CVBS signal is synchronised with the horizontal oscillator, thus whether the PHI-1 loop is in-lock. The output is available by I²C bus, **SL**, and can be used for search tuning and OSD. In automatic mode (**FOA/FOB** = 0 0) the coincidence detector switches for out of lock condition the PHI-1 loop to fast to ensure fast horizontal catching. During search tuning the coincidence detector can be made less sensitive (about 5 dB) by control bit **STM** (search tuning mode). This prevents false stops.

*** Vertical sync separator**

The vertical sync separator separates the vertical sync pulse from the composite sync signal. This separated sync pulse is used to trigger the vertical divider system. To generate a trigger pulse for the divider the minimum pulse width of the incoming vertical sync pulse must be 17µs.

The integrator network is designed such that for anticopy signals (e.g. Macrovision) with vertical pulses of 10µs (on) and 22µs (off) still a vertical sync pulse is generated. (Because more lines with vertical pulses are present, pulse width of less than 17µs is allowed, by integration still the required level is reached).

To improve the behaviour for such anticopy signals, an extra gating function is implemented to prevent disturbance of the PHI-1 loop during these extra vertical pulses. This gating function can be enabled by setting **EMG** = 1 and is only active under the following conditions:

- **EMG** = 1 (Macrovision gating enabled)
- **SL** = 1 (valid signal present)
- **IVW** = 1 (Norm or near norm signal detected, 522-528/622-628 lines/frame)

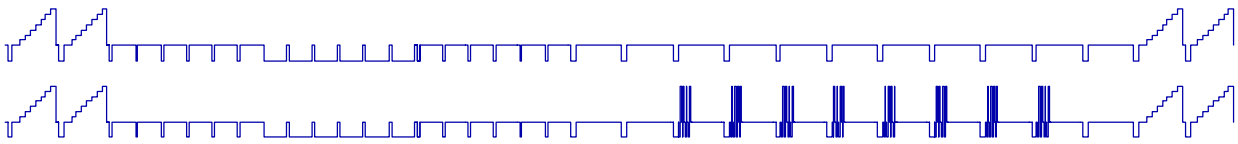


Fig 8 : Vertical synchronisation, normal (above) and with anticopy signal (below)

*** Vertical divider system**

The divider system uses a counter that delivers the timing for the vertical pulse at the VA output pin 61 The clock is derived from the horizontal line oscillator.
The divider system synchronizes on the vertical sync pulse of the vertical sync separator.

The divider has three modes of operation:

1 Search mode (large window)
This mode is activated when the circuit is not synchronized or when a non-standard signal is received.
In the search mode the divider can catch between about 45 and 64.5Hz.

2 Standard mode (narrow window)
This mode is switched on (coming from search mode) when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window (thus automatic insertion of missing vertical sync pulses). As consequence the disturbance of the picture is very small. The circuit will switch back to the search window when 6 succeeding vertical periods no sync pulses are found within the window. (See also **NCIN** below)
In the narrow window mode the PHI-1 is inhibited during the vertical egalization pulses to prevent disturbance.

3 Standard TV-norm: divider ratio 525 (60Hz) or 625 (50Hz)
When the system is switched to the narrow window (standard mode) it is checked whether the incoming vertical sync pulses are according to the TV norm, if so **IVW=1**. When 15 standard TV-norms are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.
The system switches back to the narrow window when 3 vertical sync pulses are missed. When also in the narrow window 3 vertical sync pulses are missed the divider will switch to the search window mode.

As described above the vertical divider needs some waiting time before switching back to the search window mode. When a fast reaction is required for instance during channel switching the system can be forced to the search window by means of I²C bus, setting **NCIN** = 1 (vertical divider mode). Immediate after forcing to search mode **NCIN** has to be set back to 0 for optimum performance.

The vertical synchronisation mode of operation can be selected by I²C bus, when no input signal is present (**SL** = 0), the vertical frequecny is pending on the settings of **FORF**/**FORS** (**FOR**ced **F**ield frequency):

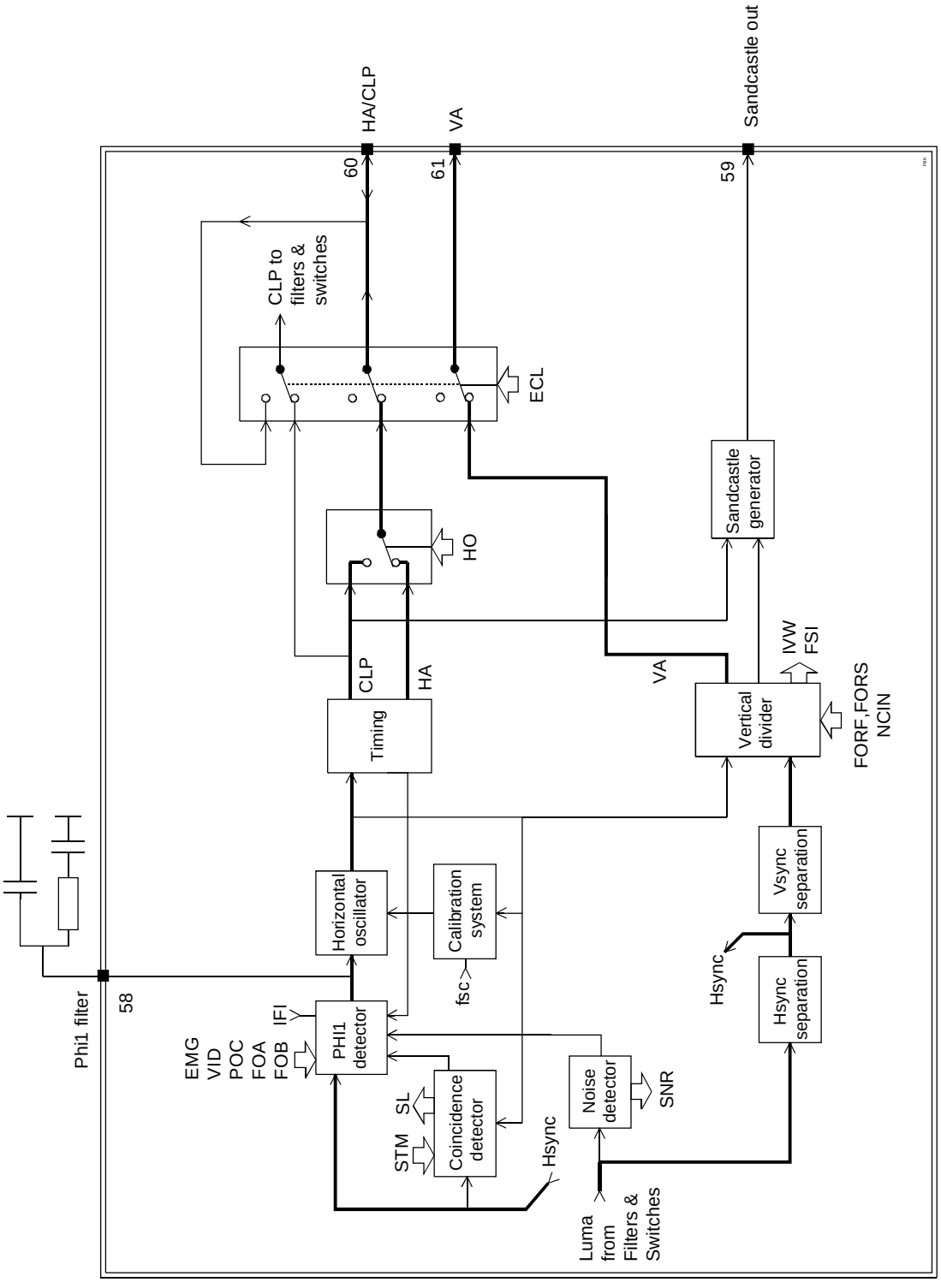
- 0 0 60 Hz when **SL** = 0, synchronizing on both 50 and 60 Hz input signals when available
- 0 1 60 Hz only, 60 Hz when **SL** = 0, synchronizing only from 54 to 64.5 Hz, for 60 Hz only environment, cannot synchronize on 50 Hz input signals (picture starts rolling)
- 1 0 Keep last detected, remains at vertical frequency of the input signal, present before **SL** becomes 0, synchronizes both on 50 and 60 Hz input signals. This mode is useful when both 50 and 60 Hz signals can be received but signal conditions are such that for short time signal (and synchronisation) is lost.
- 1 1 50 Hz when **SL** = 0, synchronizing on both 50 and 60 Hz input signals when available

Note that when **POC** is set to 1, **SL** is immediately forced to 0 and the vertical output will direct run on the frequency, selected by **FORF/FORS** for **SL** = 0.

Furthermore 50/60Hz identification is available by I²C bus **FSI** (50/60Hz), and norm signal identification with **IVW**.

*** Vertical output VA**

The vertical divider generates an output pulse for further processing of the YUV signals and for display and deflection timing.
The pulse is positive and the rising edge starts 37.7 µs after the starting edge of the vertical synchronisation in the composite sync. The duration is 2.5 lines for 50 Hz signals and 3 lines for 60 Hz signals.
When for the horizontal pin 60 external clamp mode is selected (**ECL** = 1), V_A is suppressed.



A 2 : Block diagram: Horizontal and vertical synchronization

2.2.3 Filters and Switches

See also the related block diagram A3 at page 37.

The main functions are:
* CVBS, Y/C signal selection.
* Filter calibration.
* Chrominance signal processing.
* Luminance signal processing.
* Y helper lines processing.
* YUV_{INT} and RGB/YUV_{EXT} selection.

*** CVBS, Y/C signal selection**

The input selector has 3 CVBS inputs at pins 14, 16 & 18 and 2 Y/C inputs at pins 20, 21 & 23, 24 which can be selected via the I²C bus **(DEC3..0)**; the Y/C inputs can also be used as additional CVBS inputs.
Two AV inputs are available which can be used for sensing 3 voltage levels on each pin, for instance to sense the status of pin 8 of SCART connectors. The status can be read out via I2C bus bits S1A, S1B and S2A, S2B.

For AUTO YC mode (Put **DEC3**=1), the input selector automatically detects whether a CVBS or Y/C signal has been supplied by monitoring the burst amplitude at pins 20, 21 if **DEC 3..0** is set = 1,1,0,0 (or pins 23, 24 if **DEC 3..0** is set = 1,1,1,0) once after sync lock; the larger burst signal has selection preference. The selection status can be checked with the status output bit **YC** ; (note that during search mode for the colour system then **YC** = 1).

For application with combfilters:
- **ECMB** is set = 1; the subcarrier frequency F_{SC} with DC level of 4.2V is present at pin 30.
- SYS1, SYS2 outputs at pins 25, 27 is used to switch the comb filter to the different colour standards according to Table 4 .

The selected input signal is supplied to combfilter from pin 26. For PAL/NTSC signals, the combed Y/C outputs from the combfilter (supplied to the Y_{COMB} , C_{COMB} inputs at pins 28, 29 respectively) are selected; for SECAM or BLACK-WHITE signals, the Y_{COMB}, C_{COMB} inputs at pins 28, 29 will not be selected but instead the concerned CVBS or Y/C signal remains selected.

Colour standard	SYS1	SYS2	Selected Xtal
PAL-M	0	0	C (3.575611)
PAL-B,G,H,D,I	0	1	A (4.433619)
NTSC-M	1	0	D (3.579545)
PAL-N	1	1	B (3.582056)

Table 4 : SYS1, SYS2 truth table

In AUTO COMB mode (**ECMB** and **DEC3** are both set = 1), the input selector automatically selects Y/C mode if larger burst is present at the C inputs (pins 21, 24) for all standards. If larger burst is present at the CVBS3, CVBS4 inputs then comb filter outputs (supplied to the Y_{COMB} , C_{COMB} inputs at pins 28, 29 respectively) is selected however for SECAM or BLACK-WHITE signals (i.e. combing is not possible), the concerned CVBS signal remains selected.
The selection status whether Y_{COMB} , C_{COMB} (pins 28, 29) is selected can be checked with the status output bit **CMB**.
The three outputs ($CVBSO_{TXT}$, $CVBSO_{PIP}$ and COMBCVBS) can be independently selected as shown in Table 5 to Table 7. This allows the features:

- displaying main and PIP CVBS signals independently,
- record select out,
- monitoring teletext from different source. In Y/C mode, the Y and C signals are added to form a CVBS signal and can be supplied to:

- the $CVBSO_{TXT}$ output (**TXT2..0** = 1, 0, 1 or 1, 1, 1)
- the $CVBSO_{PIP}$ output (**PIP2..0** = 1, 0, 1 or 1, 1, 1) or
- the COMBCVBS output (refer to Table 5).

Note: The names are arbitrary in that it is possible to supply COMBCVBS signal to both combfilter and teletext decoder and supply $CVSO_{TXT}$ signal to the SCART plug.
The input selector configuration is shown in Fig 9.

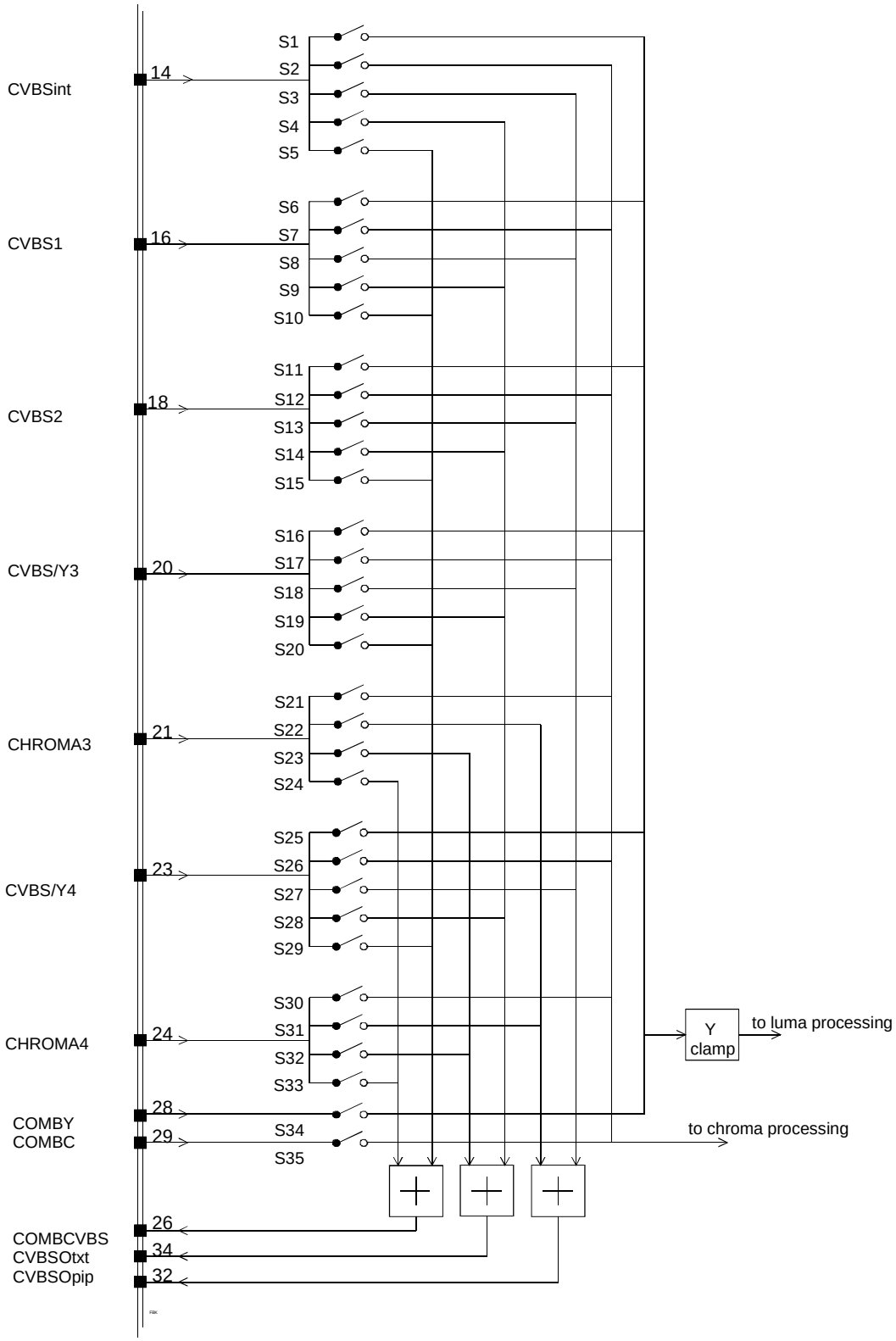


Fig 9 : Input selection

ECMB	DEC3	DEC2	DEC1	DEC0	SELECTED SIGNAL	COMBCVBS OUTPUT	CLOSED SWITCHES (refer to Fig 9)
0	0	0	0	X	CVBSint	CVBSint	S1 S2 S5
0	0	0	1	0	CVBS1	CVBS1	S6 S7 S10
0	0	0	1	1	CVBS2	CVBS2	S11 S12 S15
0	0	1	0	0	CVBS3	CVBS3	S16 S17 S20
0	0	1	0	1	YC3	Y3+C3	S16 S20 S21 S24
0	0	1	1	0	CVBS4	CVBS4	S25 S26 S29
0	0	1	1	1	YC4	Y4 +C4	S25 S29 S30 S33
0	1	1	0	0	auto YC3	CVBS3 or Y3+C3	S16 S17 S20 or S16 S20 S21 S24
0	1	1	1	0	auto YC4	CVBS4 or Y4 +C4	S25 S26 S29 or S25 S29 S30 S33
1	0	0	0	X	YC COMB	CVBSint	S5 S34 S35
1	0	0	1	0	YC COMB	CVBS1	S10 S34 S35
1	0	0	1	1	YC COMB	CVBS2	S15 S34 S35
1	0	1	0	0	YC COMB	CVBS3	S20 S34 S35
1	0	1	1	0	YC COMB	CVBS4	S29 S34 S35
1	1	1	0	0	auto COMB3	CVBS3 or Y3 +C3	S20 S34 S35 or S16 S20 S21 S24
1	1	1	1	0	auto COMB4	CVBS4 or Y4 +C4	S20 S34 S35 or S25 S29 S30 S33

Table 5 : Input selection possibilities

TXT2	TXT1	TXT0	CVBSO TXT	CLOSED SWITCHES (refer to Fig 9)
0	0	X	CVBSint	S4
0	1	0	CVBS1	S9
0	1	1	CVBS2	S14
1	0	0	CVBS3	S19
1	0	1	Y3 + C3	S19 S23
1	1	0	CVBS4	S28
1	1	1	Y4 + C4	S28 S32

Table 6 : TXT output selection possibilities

PIP2	PIP1	PIP0	CVBSO PIP	CLOSED SWITCHES (refer to Fig 9)
0	0	X	CVBSint	S3
0	1	0	CVBS1	S8
0	1	1	CVBS2	S13
1	0	0	CVBS3	S18
1	0	1	Y3 + C3	S18 S22
1	1	0	CVBS4	S27
1	1	1	Y4 + C4	S27 S31

Table 7 : PIP output selection possibilities.

*** Filter calibration**

The filter calibration loop is an auto-tuning loop which calibrates every field retrace. The loop is stabilised when the resonant frequency of the cloche filter is Fsc (Fsc = VCXO reference signal which is at 4.4MHz or 3.6MHz depending upon which Xtal is selected).

The chroma bandpass and chroma trap filters are also controlled to Fsc. The chroma bandpass centre frequency can be set to 1.1Fsc via I2C bus command **CB.**

For SECAM reception the cloche resonant frequency is set to 4.286MHz and the chroma trap is shifted to 4.3MHz to ensure optimal subcarrier rejection.

*** Chrominance signal processing**

For chroma signal processing, the selected signal is supplied to both the PAL/NTSC chroma bandpass filter and the SECAM cloche filter via a variable gain amplifier which is controlled by ACC and ACL detection circuits.

The dynamic range of the ACC is 26dB and detects only the burst amplitude; consequently the burst signal at the bandpass/cloche filter input is constant for a burst signal range +6dB -> -20dB where 0dB = 300mV$_{pp}$ burst.

The ACL is a chroma amplitude detector and is active when the chroma/burst ratio exceeds approximately 3. It ensures that CVBS signal to chroma bandpass & cloche filter is limited for large chroma/burst ratios (>3). which results in a constant saturation for such non-standard transmissions.

The ACL is independent of the ACC; it controls only the chroma amplitude and does not influence the colour burst sensitivity. The ACL function can be switched on/off via bus command **ACL**.

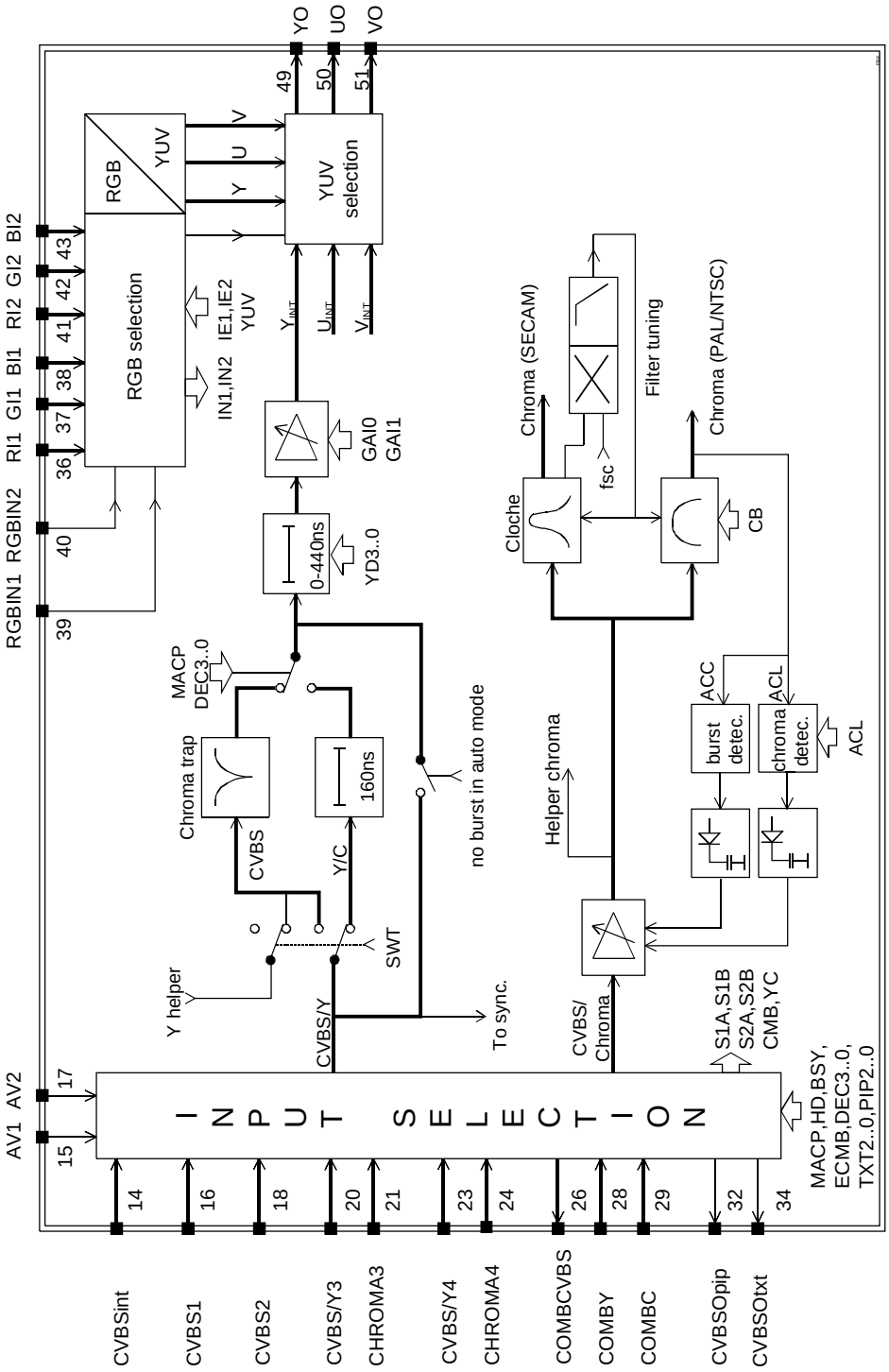
The output signal of the chroma bandpass circuit is supplied to the PAL/NTSC decoder and the output signal of the cloche filter is supplied to the SECAM decoder for further chroma processing.

For PALplus helper demodulation the chrominance signal at the input of the bandpass filter is used. This to insure sufficient bandwidth of the demodulated Y helper signal. Omitting the bandpass filter is not a problem here because the helper lines only contain chrominance information.

*** Luminance signal processing**
For luminance processing, the selected CVBS signal is first clamped and then supplied to the chroma trap circuit.
The chroma trap is bypassed for no burst transmissions when in own intelligence mode (automode).
For Y/C mode, the Y signal follows a direct path with 160ns delay so as to ensure similarity with chroma trap delay.
Consequently the Y signal is supplied to an adjustable delay line (0ns - 440ns, minimum step is 40ns, controlled via bus bits YD3..0) and variable gain circuit (I2C bus bits **GAI1** and **GAI0**) before being supplied to the YUV selection circuit.

*** Y helper lines processing.**
For PALplus mode the decoded Y helper signal from helper decoder always follows the CVBS path with chroma trap to suppress the 4.43MHz restcarrier. The helper signal is multiplexed with the regular 430 letterbox lines luminance signal. Notice that the 430 letterbox lines luminance signal not only can follow the CVBS path with chroma trap (in case of a CVBS input signal) but also the Y/C path with 160ns delay line (in case of a Y/C signal or when selecting external digital MACP processing).

*** YUV_{INT} and RGB/YUV_{EXT} selection.**
Two external linear RGB inputs with fast blanking possibility are available; fast blanking RGB2 has priority above fast blanking RGB1.The RGB1inputs can also be used as YUV inputs (selectable via I2C bus). The RGB signals are converted to YUV signals and then fed to the YUV selection circuit. Here it is possible to insert the external signals in the internal YUV picture for OSD or PIP applications. The clamping of the RGB signals is normally done with an internal clamppulse, however if the external RGB signals are not synchronous with the internal YUV signals an external clamppulse has to be supplied via pin 60 HA/CLP output/input. See also page 26, *** Horizontal input/output**.



A 3 : Block diagram: Filters and Switches

2.2.4 Colour decoder

See also the related block diagram.

The main functions are:

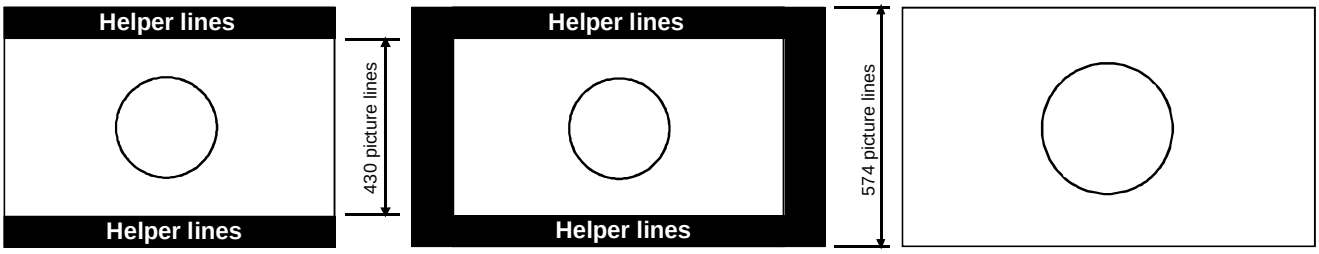
* PLL/VCXO
* PAL/NTSC demodulation
* PALplus helper demodulation
* SECAM demodulation
* ASM (Automatic System Manager)

*** PLL/VCXO**
The PLL operates during the burstkey period; it generates a VCXO reference signal (f_{VCXO}), in phaselock with the incoming burst signal (f_{BURST}).
Prior to lock condition, the signals f_{VCXO} and f_{BURST} are not synchronous and are present at phase detector input. The loop filter averages the phase detector output current and the resulting control signal to the VCXO is proportional to $Sin(2\pi\Delta ft)$ where $\Delta f = f_{VCXO} - f_{BURST}$.
A lock situation occurs when $\Delta f <$ VCXO holding range; once in lock, the phase detector output current is proportional to $\Theta_E = \Theta_{VCXO} - \Theta_{BURST}$ (Θ_E is the static phase error).
The combined phase detector and VCXO sensitivity is high to ensure a small static phase error.
For fast colour acquisition, the phase detector is in high gain mode when a colour system is not yet identified.
The VCXO loop (not to be confused with phase locked loop, PLL) compensates for any attenuation loss or phase shift in the crystal so that the it's loop gain is unity and loop phase shift is zero. The VCXO reference outputs (0° and 90°) are stable sinusoids.
VCXO oscillation is at series resonance of the selected Xtal. Since the PLL automatically tunes the VCXO to the burst (if inside the PLL holding range) fine tuning of the VCXO with a trimming capacitance is not necessary.
The motional capacitance of the Xtal is damped by the internal resistance of the VCXO pins (i.e. 1K) in order to realise the holding range.
The catching range (pull-in) of the PLL loop is governed by the PLL loop filter; the loop filter can be chosen so that PLL holding and catching range are similar (direct catching).
The HUE phase rotator is inoperational when the PLL is active (i.e no phase rotation during the burstkey period). Outside the burstkey period, the hue control rotates the VCXO reference phases from -40° to 40° linearly for I²C bus command **(HUE: 0 --> 63)**, see also device specification.

*** PAL/NTSC demodulation**
The 0° and 90° reference signals from the VCXO are supplied to the HUE phase rotator; it's outputs (H0, H90) are supplied to the (B-Y) and (R-Y) burst demodulators respectively.
The demodulated burst from the (B-Y) demodulator supplies NTSC ident information to the ASM (IDN signal).
The demodulated burst from (R-Y) demodulator supplies PAL ident information to the ASM (IDP signal).
For correct demodulation of (R-Y) PAL burst and chroma signals, then the H90 signal requires 180° phase shift on alternate lines. This is realised with the H/2 switch before the (R-Y) demodulator. It is not active during demodulation of NTSC signals.
The (B-Y)/(R-Y) baseband signals are obtained from the chroma signal by the (B-Y)/(R-Y) demodulators, filtered and supplied via the PAL/SECAM switch (PS) to the internal baseband delay line.
The demodulator gain ratio (B-Y)/(R-Y) is typically 1.78 in order to compensate for scaling in the transmitter.
For NTSC applications it is possible to bypass the delay line via I2C bus command **BPS**; the gain is also corrected then by a factor two.
The V_{INT} and U_{INT} signals from delay line outputs are fed to the YUV selection circuit (see YUV/RGB processing part).

PALplus

PALplus has been developed to introduce wide screen transmissions with a backward compatibility for PAL 4:3 sets. A PALplus signal has the format of a standard analogue PAL composite signal, containing 430 PAL picture lines in letterbox format (lines 60 - 274 and 372 - 586), together with helper information hidden in the black bands above and below the visible letterbox area (lines 24 - 59, 336 - 371, 275 - 310, 587 - 622).
A viewer with a 4:3 TV set will see a letterbox picture: black bars of 1/8 picture height at the top as well as at the bottom with a 16:9 picture in between (see Fig 10a).



PALplus signal on a 4:3 TV set

(a)

PALplus signal on a 16:9 TV set, no PALplus decoding, no zoom expand

(b)

PALplus signal on a 16:9 TV set, PALplus decoded

(c)

Fig 10 : Possible PALplus picture displays

A wide screen TV set without PALplus decoder will show a picture as in Fig 10b, or when a zoom function is available, a picture as in Fig 10c, however with only 430 lines of vertical resolution.
When a wide screen TV set has a PALplus decoder, it expands the letterbox format to a full-size wide screen picture with a vertical resolution of 574 lines. The decoder uses the helper information, hidden within the black bars.
Furthermore a PALplus signal will deliver full luminance bandwidth when using a Y/C separation technique called: 'Motion Adaptive Colour Plus' (MACP). Using this technique the signal becomes free from cross colour and cross luminance. This algorithm requires MACP preprocessing in the PALplus encoder at the studio output.
This digital MACP processing takes place on the YUV signals.

*** PALplus helper demodulation**

The Y helper synchronous demodulator uses the chroma signal before the chroma bandpass to achieve sufficient bandwidth. This demodulator is active during the helper lines when **HD = 1**. The correct B-Y demodulation axis can be adjusted via subaddress 03 (D5..D0).
The demodulated Y helper lines are multiplexed with the luminance letterbox lines (see Filters & Switches: *** Y helper lines processing**).

The PALplus parts which the TDA9321 H processes are in short:
- helper demodulation and multiplexing the helper signal with the letterbox luminance signal.
- chrominance trap bypassing if necessary.
- creation of reference line 22 (see Fig 11).
- creation of black set-up and helper set-up (see Fig 11).
- correct blanking and timing reference for the necessary PALplus post processing IC's.

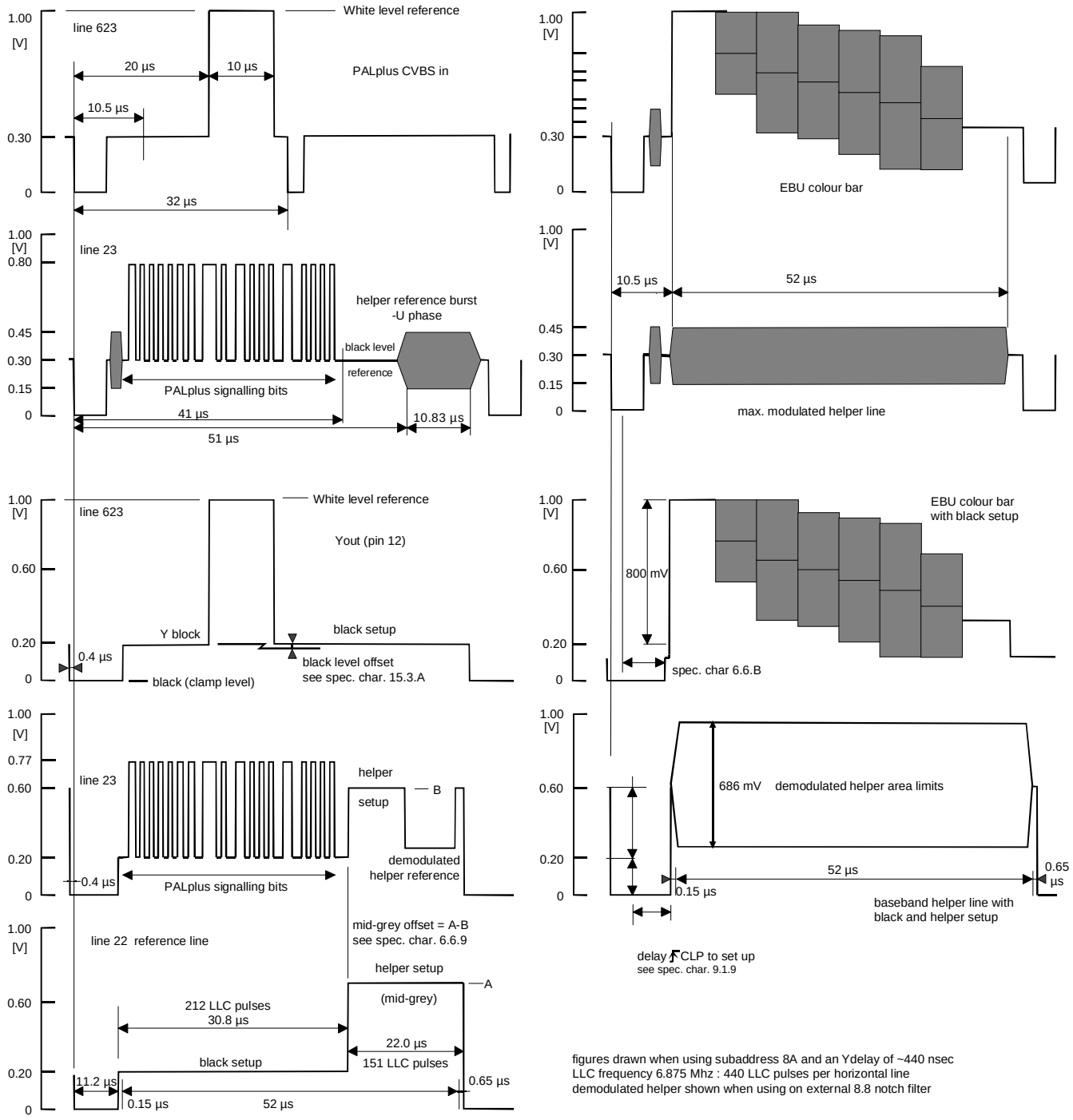
In case of a PALplus input signal, the standard identification system of the TDA9321 H only determines PAL and needs additional I^2C-bus information for PALplus processing via bus bits **MACP**, **HD**, **HOB** and **HBC**.
The **HD** bit (helper demodulation) enables PALplus helper demodulation on the U phase (i.e. the B-Y demodulation axis). The demodulated helper luminance signal is always led to the 4.43MHz notch filter,
is multiplexed with the regular 430 letterbox lines luminance signal and via the adjustable luminance delay line and YUV selection circuit supplied to the Y output. The black level of the luminance signal is internally clamped to the black level generated by the helper demodulator.
As there is only a 4.43MHz internal notch filter for the demodulated helper, an external notch filter is necessary to suppress the remaining 8.86MHz demodulation product. Using an internal low pass filter as used after the
(R-Y) and (B-Y) demodulators is not possible here on account of the high requirements needed for bandwidth and group delay of the helper luminance signal.

Bus bits **HD** and **MACP** also determine the presence of a black set-up voltage (with luminance scaling of a factor 0.8) and a helper set-up voltage for the demodulated helper signal on the Y output signal. These set-up voltages are necessary for PALplus signal post processing outside the TDA9321 H. The set-up voltages are also multiplexed into a reference line 22, used together with the demodulated helper reference of line 23 and luminance reference of line 623 both present in every PALplus signal for correct PALplus reference post processing. See Fig 11.

Additional helper blanking bits (**HOB, HBC**) determine whether the helper signal has to be blanked or blanked conditionally depending on the signal to noise ratio bit **SNR**. Helper blanking can only take place on a norm sync signal, indicated by output bit **NRM = 1** (See also page 58, **HOB** : **H**elper **O**utput **B**lanking).

The TDA9321 H can handle PALplus signals in either CVBS or Y/C format. In case of a Y/C signal the modulated helper must be available on one of the chrominance input pins. The use of the 4.43MHz trap will not be necessary then, as the chrominance and luminance component are already separated, so the 4.43MHz trap is bypassed for the letterbox luminance signal (not for the demodulated helper signal).
During helper demodulation the internal chroma bandpass filter is not used.

The signalling bits in line 23 (see Fig 11) are processed in the same manner as letterbox luminance lines.
Signalling bit decoding and PALplus identification has to be done externally with the I^2C bus as communication link to the TDA9321 H via bus bits **MACP, HD, HOB** and **HBC**.



figures drawn when using subaddress 8A and an Ydelay of ~440 nsec
LLC frequency 6.875 Mhz : 440 LLC pulses per horizontal line
demodulated helper shown when using on external 8.8 notch filter

Fig 11 : PALplus CVBS input and Y output signals

*** SECAM demodulation**

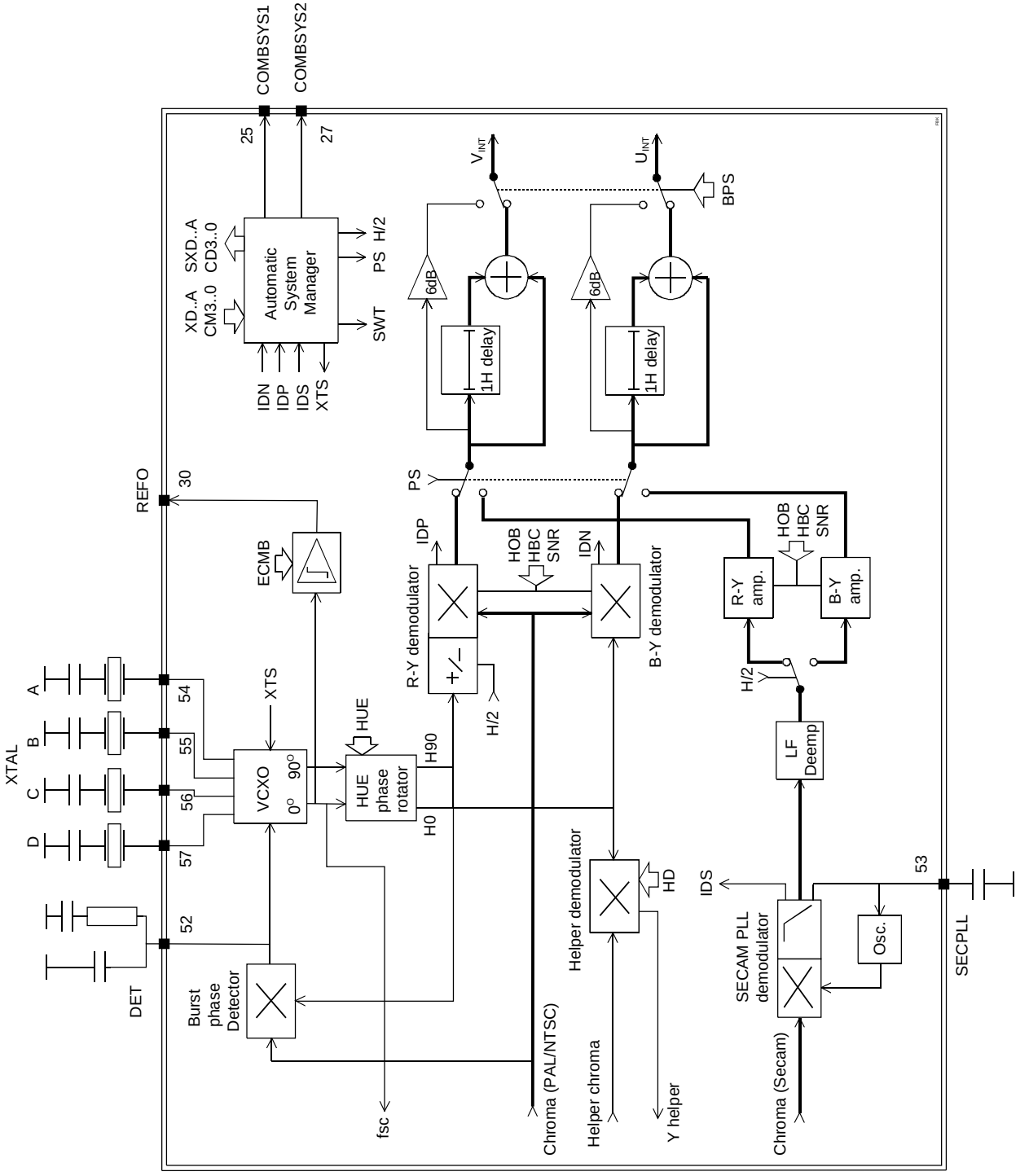
SECAM demodulation is realised with a PLL type demodulator.
If a 4.43MHz Xtal is present on pin 54 then SECAM demodulation is possible. The auto tuning loop, consisting of PLL demodulator and oscillator, ensures that the PLL oscillator is locked to the 4.43MHz Xtal frequency during calibration time in the vertical retrace period. The SECAM reference voltage, generated at pin 16, is regulated in order that the PLL demodulator output is set to a reference voltage derived from an internal stable bandgap voltage.
Outside calibration the oscillator remains tracking the SECAM chrominance resulting in the corresponding demodulated voltage. This is delivered to the LF de-emphasis stage and to the line ident stage of the Automatic System Manager (IDS signal). The H/2 switch distributes the demodulated signal to the (R-Y) and (B-Y) amplifiers and via the PAL/SECAM switch (PS) to the baseband delay line.
The V_{INT} and U_{INT} signals from delay line outputs are fed to the YUV selection circuit (see Filters & Switches).

*** ASM (Automatic System Manager)**

The ASM is field synchronous; it can identify PAL/NTSC/SECAM colour standards. The different possibilities are controlled by the I²C bus input commands **(CM3, CM2, CM1, CM0)** . These input commands are communicated to the ASM via the I²C bus.
The I²C bus input commands **(XD, XC, XB, XA)** , also supplied to the ASM via the I²C bus, indicate which Xtals are connected to pins 54, 55, 56, 57. This is also essential for correct calibration of the horizontal oscillator.
For colour identification purposes there is also communication with the ASM and:

- the PAL/NTSC ident circuits (IDP, IDN)
- the SECAM ident (IDS)
- the VCXO via Xtalswitch (XTS)
- the PAL/SECAM switch (PS)
- the R-Y demodulator (H/2)

The I²C output commands **(SXD, SXC, SXB, SXA)** indicate whether the **(XD, XC, XB, XA)** bits have been correctly transmitted by the I²C bus. The I²C output commands **(CD3, CD2, CD1, CD0)** indicate which colour system has been identified.



A 4 : Block diagram: Colour decoder

2.2.5 I²C bus description

2.2.5.1 Overview I²C bits

For easy control, most functions of the TDA9321 H are controlled via the I^2C bus:

Input functions[1)] (write)	Sub addr. (hex)	Data bits							
		D7	D6	D5	D4	D3	D2	D1	D0
Colour decoder 0	00	CM3	CM2	CM1	CM0	XD	XC	XB	XA
Colour decoder 1	01	MACP	HOB	HBC	HD	0	ACL	CB	BPS
Luminance	02	0	0	GAI1	GAI0	YD3	YD2	YD1	YD0
Hue control HUE	03	0	0	A5	A4	A3	A2	A1	A0
Spare	04	0	0	0	0	0	0	0	0
Synchronisation 0	05	FORF	FORS	FOA	FOB	0	VIM	POC	VID
Synchronisation 1	06	0	0	0	0	BSY	HO	EMG	NCIN
Spare	07	0	0	0	0	0	0	0	0
Video switches 0	08	0	0	0	ECMB	DEC3	DEC2	DEC1	DEC0
Video switches 1	09	0	PIP2	PIP1	PIP0	0	TXT2	TXT1	TXT0
RGB switch	0A	0	0	0	0	YUV	ECL	IE2	IE1
Output pin switches	0B	0	0	0	0	0	0	OS1	OS0
Vision IF	0C	FFI	IFO	GD	MOD	AFW	IFS	STM	VSW
Tuner take-over	0D	0	0	A5	A4	A3	A2	A1	A0
Adjustment IF PLL	0E	L'FA	A6	A5	A4	A3	A2	A1	A0
Output (read)		Data bits							
Status byte 0	00	POR	x	x	x	SNR	FSI	SL	IVW
Status byte 1	01	CD3	CD2	CD1	CD0	SXD	SXC	SXB	SXA
Status byte 2	02	IN1	IN2	CMB	YC	S2A	S2B	S1A	S1B
Status byte 3	02	ID3	ID2	ID1	ID0	IFI	PL	AFA	AFB

Table 8 : Condition PHI-1 loop

1) Note: All not-used bits should be set to zero, for compatibility with future devices.

For quick reference are all bits listed in alphabetical order in the two tables below. The bits are split up for control functions and analogue control.:
The meaning of the different colums in the table are:

Control bits table:

CONTROL BIT	The short name for the control bit
FUNCTION	A short functional description
REG	The register subadress in HEX.
BIT	The bit number (D7..D0) in the register
I/O	Input or Output, Input = control bit, Output = status bit
MACRO	The device macro, where the bit is related to: IF: Vision IF Sound: Sound part Sync: Horizontal and Vertical synchronisation Geo: Geometry (vertical & horizontal) and drive of vertical deflection Filt/Sw: Filters and CVBS/Y/C switches Col.Dec. Colour decoder RGB: RGB output, input and control
FU	Function class, the bits are divided in 5 classes: SU **S**tart-**U**p, bit has to be set correct before switching on from stand-by. AL **Al**ignment, bit(s) have to be aligned during production, the found values are set each time before switching on from stand-by SC **S**etmaker **C**ontrol, bits which have to be controlled by the setmaker during operation for correct performance like PHI-l loop time constant, positive modulation, etc. UC **U**ser **C**ontrol, bits which are normally accessible for the customer like contrast, brightness, etc. TK **T**ool **K**it, bits which can help to improve performance under difficult working conditions like RF phase modulation, wrong burst/chroma ratio, etc.

Analog control:
Most colums are identical. The deviating colums:

STEPS	The number of steps, available for this analogue function
RANGE	The control range of the analogue control.

Survey control bits, in alfabetical order of their abbriviated name

CONTROL BIT	FUNCTION	REG	BIT	I/O	MACRO	FU
ACL	**A**utomatic **C**olour **L**imiting, 1=on	01	2	I	Filt/Sw	TK
AFA, AFB	**AF**C outputs	03	1,0	O	IF	SC
AFW	**AF**C **W**indow, 1=275 kHz	0C	3	I	IF	SC
BPS	**B**y**P**a**S**s base band delay line, 1=bypassed	01	0	I	Col.Dec.	SC
BSY	**B**lanked **S**ync on **Y**-output, 1 = blanked	06	3	I	Filt/Sw	SC
CB	**C**entre frequency chroma **B**andpass, 0=centre freq.=Fsc, 1=centre freq.=1.1 Fsc	01	1	I	Filt/Sw	SC
CD3..0	**C**olour **D**etection	01	7,6,5,4	O	Col.Dec.	SC
CM3..0	**C**olour decoder **M**ode	00	7,6,5,4	I	Col.Dec.	SC
CMB	Condition Y/C input for **C**o**MB** filter, 0 = CVBS at comb-filter input selected, 1 = Y/C input for combfilter out selected	02	5	O	Filt/Sw	SC
DEC3..0	Colour **DEC**oder input	08	3,2,1,0	I	Filt/Sw	UC
ECL	**E**xternal **Cl**amp pulse mode, 1 = use external clamp pulse	0A	2	I	Sync	SC
ECMB	**E**nable **C**o**MB** filter mode, 1 = subcarrier present on pin 30 and selection of Y/C combfilter input when CVBS fed to combfilter input can be combed	08	4	I	Filt/Sw	SC
EMG	**E**nable **M**acrovision **G**ating, 1 = enabled	06	1	I	Sync	SC
FFI	**F**ast **F**ilter **I**F-PLL, 0=normal, 1=fast time constant	0C	7	I	IF	TK
FOA, FOB	**Fo**rced ϕ1 time constant	05	5,4	I	Sync	SC
FORF, FORS	**FOR**ced **F**ield frequency	05	7,6	I	Sync	SC
FSI	**F**ield **S**ynchronisation **I**ndication, 1=60 Hz, 0=50 Hz	00	2	O	Sync	SC
GD	**G**roup **D**elay, 0 = flat, 1 = B/G standard	0C	5	I	IF	SC
HBC	**H**elper **B**lanking **C**onditional, 1 = pending on SNR bit	01	5	I	Col.Dec.	SC
HD	Pal-plus **H**elper **D**emodulation, 1 = on with helper / black set-up of 400 / 200 mV	01	4	I	Col.Dec.	SC
HO	**H**orizontal **O**utput signal pin 60, 0 = CLP, 1 = H_A	06	2	I	Sync	SU
HOB	**H**elper **O**utput **B**lanking for PAL plus, 1=on, see also HBC	01	6	I	Col.Dec.	SC
ID3..0	Device **ID**entification code	03	7,6,5,4	O	DevSel	SC
IE1, IE2	**I**nsertion **E**nable fast blanking RGB input **1**, **2**, 1=enabled	0A	0,1	I	Filt/Sw	SC
IFI	Output of video (**IF**-) **I**dent circuit, 1=video identified	03	3	O	IF	SC
IFO	**IF** amplifier **O**peration, 0 = normal, 1 = switched off	0C	6	I	IF	SC
IFS	**IF S**ensitivity, 1=low sensitivity	0C	2	I	IF	SC
IN1, IN2	Reflects the level on the fast blanking **IN**put pin of RGB **1**,**2** in (pin 39,40), 1 = insertion active	02	7,6	O	Filt/Sw	SC
IVW	**I**n **V**ertical divider **W**indow, 1=522-528/622-628 lines/frame, 0=no standard	00	0	O	Sync	SC
L'FA	**L**' **F**r**A**nce, 0=normal IF freq., 1=5.5 Mhz shifted IF freq. L'	0E	7	I	IF	SC
MACP	**M**otion **A**daptive **C**olour **P**lus mode, 0 = internal 4.43 MHz trap used, 1 = external MACP chroma filtering used	01	7	I	Filt/Sw	SC
MOD	**MOD**ulation standard, 1=positive	0C	4	I	IF	SC
NCIN	Vertical divider mode, 1=forced large window	06	0	I	Sync	SC
OS1, OS0	**O**utput pin **S**witches (pin 19, 22), 0=low level, 1=high level	0B	1,0	I	IF	SC
PIP2..0	**PIP** CVBS output selection	09	6,5,4	I	Filt/Sw	UC
PL	**P**LL -**L**ock, 1 = IF PLL in lock	03	2	O	IF	SC
POC	**P**hi-**O**ne **C**ontrol synchronisation mode, 1=loop switched off	05	1	I	Sync	SC
POR	**P**ower **O**n **R**eset, 1=failure detected	00	7	O	Pow/Prot	SC

Survey Control bits, in alfabetical order of their abbreviated name (continued)

CONTROL BIT	FUNCTION	REG	BIT	I/O	MACRO	FU
S1A, S1B	**S**tatus (DC level) on **A**V-1 input (pin 15)	02	1,0	O	Filt/Sw	SC
S2A, S2B	**S**tatus (DC level) on **A**V-2 input (pin 17)	02	3,2	O	Filt/Sw	SC
SL	**S**ync in **L**ock, 1=ϕ1-loop locked	00	1	O	Sync	SC
SNR	**S**ignal to **N**oise **R**atio of sync signal, 0 = S/N > 20 dB, 1 = S/N < 20 dB	00	3	O	Sync	SC
STM	**S**earch-**T**uning **M**ode, 1=less sensitive coincidence detector	0C	1	I	Sync	SC
SXD..A	**S**tatus of **X**-tal indication	01	3,2,1,0	O	Col.Dec.	SU
TXT2..0	**TXT** CVBS output selection	09	2,1,0	I	Filt/Sw	UC
VID	**V**ideo **ID**ent mode, 1=no influence, 0=IFI controls ϕ1-loop	05	0	I	Sync	SC
VIM	**V**ideo **I**dent **M**ode, 1=coupled to source switch output, 0 = coupled to $cvbs_{intern}$ (CVBS INT) input	05	2	I	Sync	SC
VSW	**V**ideo mute **SW**itch, 1=mute IF video out (IFVO, pin 10)	0C	0	I	IF	SC
XD..A	Definition of connected **X**-tals	00	3,2,1,0	I	Col.Dec.	SU
YC	Indication of **Y/C** on CVBS/YC inputs, 0=CVBS, 1=YC	02	4	O	Filt/Sw	SC
YUV	Selection RGB1 input function, 0 = RGB, 1 = YUV	0A	3	I	Filt/Sw	SU

Survey analogue controls, sorted in alfabetical order of abbreviated name

The parameters in the table below are just rough indications and may change without notice. Please consult the TDA9321 H data sheet (ref.[1]) for the most up-to-date values.

CONTROL	FUNCTION	REG	BIT	STEPS	RANGE	MACRO	FU
GAI1, GAI0	**GAI**n Y-output pin 49	02	5,4	4	-2 .. +1 dB	Filt/Sw	AL
HUE	**HUE** control	03	5..0	63	-40 .. +40 °	Col. Dec.	UC
IFPL	Alignment **IF**-**PL**L	0E	6..0	128	-1.85..+1.85 MHz[1)]	IF.	AL
TOP	AGC-**T**ake **O**ver **P**oint	0D	5..0	63	0.4 .. 150 mV	IF	AL
YD3..0	**Y**-**D**elay adjustment	02	3..0	12	0 .. 440 ns	Filt/Sw.	AL

Note: [1)] Resolution is better than 33 kHz per step, PLL frequency range is 32 .. 60 MHz

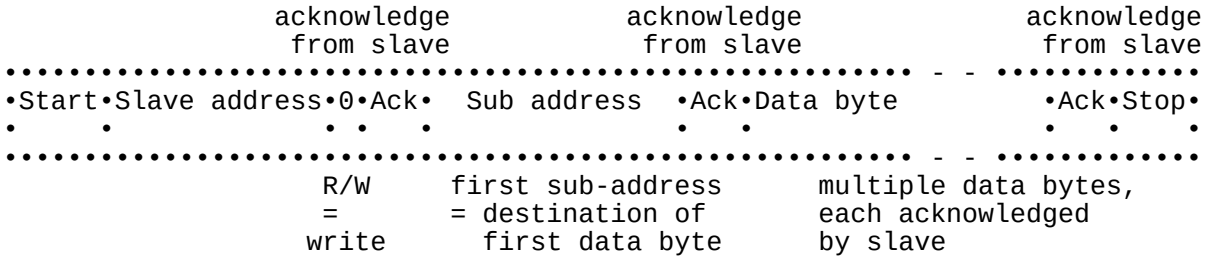
The TDA9321 H has option for two I2C device adresses. The adress is pending on the level on pin 48 (AS, Adress Select), the level on pin 48 controls the value of bit A1 of the adress:

Pin 48 grounded or open (internal pull-down resistor present): adress = $8A_{HEX}$ A1 = 0
Pin 48 connected to + 8 Volt: adress = $8E_{HEX}$ A1 = 1

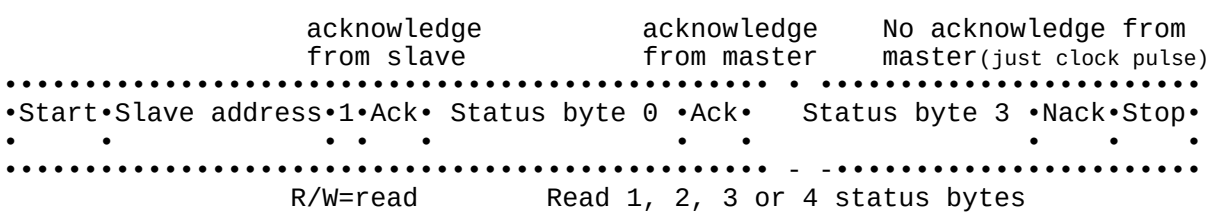
The TDA9321 H needs only two I²C-bus pins (7=SDA and 8=SCL) to read and write all its functions:

- Write slave address: $8A_{HEX}/8E_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W: 1 0 0 0 1 $^0/_1$ 1 0
- Read slave address: $8B_{HEX}/8F_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W: 1 0 0 0 1 $^0/_1$ 1 1

For I²C-bus write-transmissions the TDA884X has automatic sub-address increment, so multiple data bytes can be sent in one transmission.



Reading the four status bytes is done **without sub-addressing**. After receiving the I²C-bus read address, the TDA9321 H always starts with status byte 0.



2.2.5.2 I²C-bus start-up procedure.

The TDA9321 H has many alignment-free internal circuits that are calibrated with the frequency of the colour Xtal oscillator. With TDA9321 H an I²C-bus write-message has to tell if Xtals are connected to pins 54 to 57 (bits **XA** to **XD**). Validity of this selection is essential, therefore the following start-up procedure should be implemented in the software:

- •1 Keep reading the I²C-bus status bytes, until **POR**=0
- •2 Write all sub-address bytes including control bits **XA** .. **XD** (up till including register 0E)
- •3 Read back the Xtal setting via status bits **SXA** .. **SXD**
- •4 If (**XA** = **SXA**) .. (**XD** = **SXD**) then go to normal operation
  Else start again from point •1

After power-up, all registers must be loaded. Bits, not defined, must be loaded with zero's for future compatability. After the last sub-address is loaded, the horizontal oscillator is calibrated and the H_A/CLP output is released..

Each time before the sub-address bytes are refreshed, the status bytes must be read. If **POR**=1 then the start-up procedure must be carried out to restart the IC. Not following this procedure may result in undesired conditions after power-up or a power dip (e.g. incorrect horizontal line frequency).

2.2.5.3 IF part.

Input control bits:

AFW : **AF**C **W**indow Reg: 0C Bit: 3 Fu: SC
AFC window around IF center frequency: (useful to optimise search-tuning speed, see also output bits **AFA** and **AFB**).
0 = Nominal window, about 125 kHz wide
1 = Enlarged window, about 275 kHz wide

FFI : **F**ast **F**ilter **I**F-PLL Reg: 0C Bit: 7 Fu: TK
Fast filter IF-PLL
0= normal time constant
1= fast time constant for special market areas

This function has been made available to handle RF-transmitter signals with phase modulation. The standard loopfilter of 390E/100nF is recommended for both settings of **FFI**.

L'FA : PLL demodulator L' frequency shift Reg: 0E Bit: 7 Fu: SU
0 = normal IF-frequency
1 = IF frequency shifted for L' standard (align with D6-D0)

IFS : **IF S**ensitivity Reg: 0C Bit: 2 Fu: SC
When switched to an external source, the cross talk of noise on the internal signal to the external signal can be reduced.This function is mainly intended for no-antenna input conditions.
0 = Normal sensitivity
1 = Maximum gain reduced by 20 dB (reduces the total gain range)

MOD : **MOD**ulation standard Reg: 0C Bit: 4 Fu: SC
0 = Negative modulation
1 = Positive modulation

STM : **S**earch-**T**uning **M**ode Reg: 0C Bit: 1 Fu: SC
Can make the coincidence detector less sensitive, to avoid that search tuning systems stop at very weak signals (output bit **SL**).
0 = Normal operation
1 = Reduced dynamic sensitivity of coincidence detector (approx. 5 dB)

VIM : **V**ideo **I**dent **M**ode Reg: 05 Bit: 2 Fu: SC
Selects source for output bit **IFI** (see also **VID**, page 61, 64).
0 = Video ident circuit coupled to $CVBS1_{INT}$ (and functions are available)
1 = Video ident coupled to selected CVBS or Y/C (see **INA**, **INB**, **INC**)
Then also **IFI**=0 if **VIM**=0

VSW : **V**ideo mute **Sw**itch Reg: 0C Bit: 0 Fu: SC
When this bit is set to high, it is possible to use the internal CVBS input pin 16 ($CVBS1_{INT}$) to supply an external CVBS signal.
0 = Normal operation
1 = IF video signal switched off (pin 10 and 62 are forced to ground)
Then also **IFI**=0 if **VIM**=0

IFO : **IF** switched **o**ff circuit Reg: 0C Bit: 6 Fu: SU
In case the IF-part is not used, power consumption can be minimised.
0 = Normal operation of IF amplifier
1 = IF amplifier switched off, for minimal power consumption

GD : **G**roup **D**elay correction Reg: 0C Bit: 5 Fu: SC
Provides optimal performance in multistandard applications while a flat SAW filter is used.
0 = flat
1 = according to BG standard

OS0, OS1 : **O**utput **S**witches Reg: 0B Bit: 1/0 Fu: SC
Two output control ports OS0 and OS1 are available for external use: e.g. sound filter, SAW switching.
0 = output “low”
1 = output “high”

Output control bits:

AFA, AFB : **AF**C outputs Reg: 03 Bit: 1,0 Fu: SC
The AFC reference isthe IF-center frequency. Note: The AFC is valid when **PL**=1 only.
AFA 0 = Outside window (see **AFW** bit)
1 = Inside window
AFB 0 = Below reference, increase tuner frequency
1 = Above reference, decrease tuner frequency

IFI : Output of video (**IF**-) **I**dent circuit Reg: 01 Bit: 4 Fu: SC
Detects video at IF or selected source (see **VIM** bit).
0 = No video signal identified
1 = Video signal identified

PL : **P**LL-**L**ock Reg: 03 Bit: 2 Fu: SC
The lock bit becomes one when the PLL is in-lock, undependent upon video contents.
PL 0 = PLL not locked
1 = PLL locked

Analogue control:

TOP : AGC **T**ake **O**ver **P**oint Reg: 0D Bit: 5..0 Fu: AL
Nr. of steps: 63
Range: 0.4 .. 150 mV

Adj IF-PLL : Adjust IF-PLL Reg: 0E Bit: 6..0 Fu: AL
Nr. of steps: 127
Range: 3.7MHz, 29kHz/step

2.2.5.4 Horizontal & Vertical synchronisation

Input control bits:

ECL : **E**xternal **Cl**amp pulse mode Reg: 0A Bit: 2 Fu: SC

This bit controls the function of the H_A/CLP pin 60.

0 = Pin 60 is output, internal H_A/CLP pulse fed to pin 60.
Bit **HO** determines wether H_A or CLP pulse is selected.

1 = Pin 60 is input. External CLP pulse is used for clamping YUV/RGB inputs

When using this mode, please take the following into account:

- When ECL = 1, the external CLP pulse has also to be used for further processing of the YUV output signals
- It is practical to select in internal mode also CLP and not H_A using **HO** to allow easier processing of the YUV output signals when switching between external and internal CLP pulse mode.

EMG : **E**nable **M**acrovision **G**ating Reg: 06 Bit: 1 Fu: SC

This bit switches on the macrovision gating. This gating ensures better performance for playback of VCR tapes with Macrovision Copy Protection and prevents distortion at the top of the screen. The gating is only active when also **SL** = 1 (valid input signal present) and **IVW** = 1 (522-528/622-628 lines/frame)

0 = Macrovision gating off
1 = Macrovision gating on

FOA, FOB : **F**orced Phi-**O**ne time constant Reg: 05 Bit: 5,4 Fu: SC

These two bits determine the speed of the ϕ1-loop. It can be forced to slow and fast or set it in the automatic mode. In auto mode a noise detector circuit can switch to slow time constant, when the signal has too much noise.

FOA	FOB	ϕ1-loop mode
0	0	Auto, ϕ1-gating in slow mode [1)]
0	1	Slow, always gating (only for test purposes.)
1	0	Slow/fast depends on noise detector, always gating
1	1	Fast, no gating

Note [1)] Not suitable for weak video recorder signals, because of active ϕ1-gating in the slow mode. Use **FOA**, **FOB**=1,1 instead.

FORF/FORS : **FOR**ced field frequency Reg: 05 Bit: 7,6 Fu: SC

This forces the vertical divider in a 60 Hz mode or automatic. In auto mode it can be given a preference for 50 or 60 Hz or to keep the last detected field frequency.

FORF	FORS	Vertical frequency
0	0	Auto, 60 Hz if not locked
0	1	60 Hz forced[1)]
1	0	Auto, keep last detected frequency
1	1	Auto, 50 Hz if not locked

Note: [1)] 60 Hz is immediately forced after writing **FORF, FORS**, so when a 50 Hz signal is present, it will start rolling.

HO : **H**orizontal **O**utput mode Reg: 06 Bit: 2 Fu: SC

This bit selects the pulse fed to the horizontal output pin 60. Pending on the further video processing of the YUV output signals, selection can be made between H_A pulse (related to sync pulse) or CLP pulse (related to burstkey pulse). For timing info on both pulses, see the chapter covering synchronisation in the application description.

0 = CLP (clamp) pulse selected on horizontal output
1 = H_A pulse selected on horizontal output

NCIN : **N**o vertical **C**o**IN**cidence Reg: 06 Bit: 0 Fu: SC

Vertical divider mode: This forces the vertical divider immediately to the search window, to speed up vertical catching at channel change (it saves the time for the vertical divider to switch back from standard mode to narrow window and from narrow window to search window, which takes at least 6 fields) .
For optimal performance, NCIN should be set back to 0 after forcing the vertical divider to the search window.

0 = Normal operation of the vertical divider
1 = Vertical divider switched to search window

POC : **P**hi-**O**ne **C**ontrol Reg: 05 Bit: 1 Fu: SC

When this bit is switched to high, the ϕ1-loop is switched off completely.
In this mode very stable OSD or TEXT can be displayed, independent of the selected source. Useful for e.g. installation menu's, blue mute. It is also possible to measure the free running frequency in this way.
When forcing **POC** = 1, immediately **SL** is forced 0. This has the following consequences:

- AFC information is disabled
- Vertical divider switches immediately to mode, set by **FORF/FORS**
- **SL** cannot be used to detect a valid CVBS signal on the selected input. For this purpose, **IFI** has to be used.

For stable OSD during search tuning, it is better to use **VID** in stead of **POC**, see below..

0 = Synchronisation active
1 = Synchronisation not active

STM : **S**earch **T**uning **M**ode Reg: 0C Bit: 1 Fu: SC

With this bit it is possible to reduce the sensitivity of **SL**. This can prevent too many false stops during tuner search mode. If **STM** has to be used is pending on the expected signal conditions (many weak signals or not), the performance of the tuner and the used search algorithm.

0 = normal operation
1 = reduced sensitivity of video ident circuit **SL**

VID : **V**ideo **ID**ent coupling Reg: 05 Bit: 0 Fu: SC

With this bit it is possible to activate a coupling between video ident (**IFI**) and ϕ1-loop.
If this coupling is active and no video is present (**IFI** = 0), the ϕ1-loop is switched to very slow. This assures a stable OSD display under noisy conditions e.g. during search tuning or when no antenna input is connected (tuner noise).

0 = Video ident (**IFI**) switches ϕ1-loop on/off
1 = No influence of the video ident (**IFI**) on the ϕ1-loop

VIM : **V**ideo **I**dent **M**ode Reg: 05 Bit 2 Fu: SC

The IF ident circuit (output **IFI**) can be connected to the internal CVBS input ($CVBS_{INT}$) or after the input selection switch to the selected video input for display.

0 = **IFI** connected to $CVBS_{INT}$
1 = **IFI** connected to selected CVBS

Output control bits:

FSI : **F**ield **S**ynchronisation **I**nformation Reg: 00 Bit: 2 Fu: SC
Field frequency indication of the selected CVBS signal
0 = 50 Hz
1 = 60 Hz

IVW : **I**n **V**ertical **W**indow Reg: 00 Bit: 0 Fu: SC
Condition vertical divider window:
0 = No standard video signal detected
1 = Standard video signal detected, 522-528 or 622-628 lines/frame, vertical divider in narrow window or standard mode

SL : **S**ync **L**ock Reg: 00 Bit: 1 Fu: SC
Horizontal lock indication:
0 = Not locked
1 = ϕ1-loop locked to the incoming video signal

SNR : **S**ignal to **N**oise **R**atio Reg: 00 Bit: 3 Fu: SC
The signal to noise ratio of the selected video signal is measured during the sync pulse
0 = Signal to noise ratio > 20 dB
1 = Signal to noise ratio < 20 dB

2.2.5.5 Filters and switches

Input control bits:

ACL : **A**utomatic **C**olour **L**imiting Reg: 01 Bit: 2 Fu: TK

For signals with very large chroma/burst ratio this ACL can be enabled to maintain correct colour saturation. ACL has no influence on colour sensitivity (e.g. colour loss in VCR feature mode). It is not recommended to use the ACL function when SECAM is identified.

0 = ACL function not enabled (for standard burst/chroma transmissions)
1 = ACL function enabled (for non-standard burst/chroma ratio)

BSY : **B**lanked **S**ync on **Y** out Reg: 06 Bit: 3 Fu: TK

0 = sync pulses present on Y output
1 = blanked sync mode

During vertical and horizontal sync time the black level is filled-in.

CB : **C**hroma **B**and pass centre freq. Reg: 01 Bit: 1 Fu: SC

To compensate for the roll-off at higher frequency in the SAW filter / IF part, the centre frequency of the chroma bandpass can be shifted upwards.

0 = Centre frequency at Fsc (chroma subcarrier frequency)
1 = Centre frequency at 1.1 x Fsc (in principle used for internal mode only)

DEC3..DEC0 : Colour **DEC**oder input Reg: 08 Bit: 3,2,1,0 Fu: SC

Selected source in combination with ECMB bit:

ECMB	DEC3	DEC2	DEC1	DEC0	SELECTED SIGNAL	COMBCVBS OUTPUT
0	0	0	0	X	CVBSint	CVBSint
0	0	0	1	0	CVBS1	CVBS1
0	0	0	1	1	CVBS2	CVBS2
0	0	1	0	0	CVBS3	CVBS3
0	0	1	0	1	YC3	Y3 + C3
0	0	1	1	0	CVBS4	CVBS4
0	0	1	1	1	YC4	Y4 + C4
0	1	1	0	0	AUTO YC3	CVBS3 or Y3 + C3
0	1	1	1	0	AUTO YC4	CVBS4 or Y4 + C4
1	0	0	0	X	YC COMB	CVBSint
1	0	0	1	0	YC COMB	CVBS1
1	0	0	1	1	YC COMB	CVBS2
1	0	1	0	0	YC COMB	CVBS3
1	0	1	1	0	YC COMB	CVBS4
1	1	1	0	0	AUTO COMB3	CVBS3 or Y3 + C3
1	1	1	1	0	AUTO COMB4	CVBS4 or Y4 + C4

ECMB : **E**nable **C**o**MB** filter Reg: 08 Bit: 4 Fu: SC

0 = output pin 30 is low, no subcarrier available
1 = output pin 30 is 4.2VDC, subcarrier available

Also the YC output signals from combfilter are selected now (only if a colour standard is detected that can be combed).

GAI1, GAI0 : Luminance **GAI**n Control Reg: 02 Bit: 5,4 Fu: SC

With these bits the it is possible to adjust the gain of the luminance channel. This can be helpful to equalize the luminance levels of internal CVBS and external RGB signals.

GAI1	GAI0	GAIN
0	0	- 1dB
0	1	0dB
1	0	+ 1dB
1	1	+ 2dB

IE2, IE1 : **I**nsertion **E**nable **2**, **1** Reg: 0A Bit: 1,0 Fu: SC

Via these bits the (fast) blanking input pins 40, 39 can be made active or not.
When not active the voltage on pins 40, 39 can not influence the selection of the external RGB inputs. Always YUV internal is selected is this case.
When enabled, the selection of the YUV signals depends on the status of the blanking inputs pins 40, 39.

0 = fast blanking is not possible
1 = fast blanking is enabled

MACP : **M**otion **A**daptive **C**olour **P**lus Reg: 01 Bit: 7 Fu: SC

0 = internal 4.43MHz chroma trap is used
1 = external MACP chrominance filtering is used

At **MACP = 1** and in combination with output bit **NRM = 1**, the internal 4.43MHz chrominance trap in the luminance channel is bypassed (path Y/C in the block diagram Filters & Switches).
Also in this situation the **ECMB** bit is forced to zero (comb filter disabled). Now external digital MACP processing on the Yout signal can take place. Also a reference line 22 with set-up voltages is created and a black set-up of 200mV is added to the complete Yout signal including luminance scaling from 1.0Vbl-wh to 0.8Vbl-wh. This set-up/scaling prevents distortion of the chrominance component in the Yout signal, when supplying this signal to the external ADC's, used in a complete PALplus concept (see also page 41 **Fig 11**).

PIP2..PIP0 : **PIP** output selection Reg: 09 Bit: 6,5,4 Fu: SC
Source selection of the PIP output pin 32:

PIP2	PIP1	PIP0	pin 32 output signal
0	0	X	CVBSint
0	1	0	CVBS1
0	1	1	CVBS2
1	0	0	CVBS3
1	0	1	Y3 + C3
1	1	0	CVBS4
1	1	1	Y4 + C4

TXT2..TXT0 : **TXT** output selection Reg: 09 Bit: 2,1,0 Fu: SC
Source selection of the TXT output pin 34:

TXT2	TXT1	TXT0	pin 32 output signal
0	0	X	CVBSint
0	1	0	CVBS1
0	1	1	CVBS2
1	0	0	CVBS3
1	0	1	Y3 + C3
1	1	0	CVBS4
1	1	1	Y4 + C4

YD3..YD0 : **Y-D**elay adjustment Reg: 1A Bit: 7..4 Fu: AL
This function is meant to adjust the delay of the luminance signal to the same delay that the chroma signals U and V have because of the chroma decoding

Delay (ns) = YD3 x 160 + YD2 x 160 + YD1 x 80 + YD0 x 40 ns.

YD3	YD2	YD1	YD0	Delay setting
0	0	0	0	0 ns
0	0	0	1	40 ns
0	0	1	0	80 ns
0	0	1	1	120 ns
0	1	0	0	160 ns
0	1	0	1	200 ns
0	1	1	0	240 ns
0	1	1	1	280 ns
1	1	0	0	320ns
1	1	0	1	360ns
1	1	1	0	400ns
1	1	1	1	440 ns

YUV : **YUV**/RGB input switch Reg: 0A Bit: 3 Fu: SC

Switches the pins 36,37,38 for use as RGB inputs or YUV inputs.
0 = RGB1 inputs active
1 = YUV inputs active

Output control bits:

CMB : **C**o**MB** filter selection Reg: 02 Bit: 5 Fu: SC

Indicates if YC signals coming from combfilter are selected or not (ECMB must be 1)
0 = YC comb inputs not selected
1 = YC comb inputs selected

IN1, IN2 : Indication RGB **IN**sertion **1, 2** Reg: 02 Bit: 7,6 Fu: SC

IN1, IN2	CONDITION
0	no RGB insertion
1	full RGB insertion

S1A, S1B : **S**tatus on AV-1 input Reg: 02 Bit: 1,0 Fu: SC

S1A	S1B	STATUS	typ. DC level pin 15
0	0	no external source	0 V
0	1	4 : 3 input signal	5.5 V
1	0	16 : 9 input signal	2.2 V

S2A, S2B : **S**tatus on AV-2 input Reg: 02 Bit: 3,2 Fu: SC

S2A	S2B	STATUS	typ. DC level pin 17
0	0	no external source	0 V
0	1	4 : 3 input signal	5.5 V
1	0	16 : 9 input signal	2.2 V

YC : **YC**/CVBS input signal condition Reg: 02 Bit: 4 Fu: SC
0 = CVBS signal present on input
1 = YC signal present on input
After sync lock the decision is made once if the largest chroma burst signal is present on the C input or CVBS input. During colour search the YC bit will be "1".

2.2.5.6 Colour decoder.

Input control bits:

BPS : **By**-**P**-a-**S**-s Chroma Delay line Reg: 01 Bit: 0 Fu: SC
When active then the U, V signals bypass the built-in base band chroma delay line (e.g. for NTSC or PALplus) and are internally amplified by 6 dB to correct the levels.
0 = Baseband chroma delay line active
1 = Bypass baseband chroma delay line

CM3..CM0 : **C**olour decoder **M**ode Reg: 00 Bit: 7..0 Fu: SC
With these bits one of the automatic modes can be selected or the decoder can be forced to one of the standards.

CM3	CM2	CM1	CM0	Colour decoder mode	selected Xtal
0	0	0	0	PAL/NTSC/SECAM (auto)	A
0	0	0	1	PAL/NTSC (auto)	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	A
0	1	0	0	SECAM	A
0	1	0	1	PAL/NTSC (auto)	B
0	1	1	0	PAL	B
0	1	1	1	NTSC	B
1	0	0	0	PAL/NTSC/SECAM (auto)	ABCD
1	0	0	1	PAL/NTSC (auto)	C
1	0	1	0	PAL	C
1	0	1	1	NTSC	C
1	1	0	0	spare	
1	1	0	1	PAL/NTSC (auto)	D
1	1	1	0	PAL	D
1	1	1	1	NTSC	D

ECMB : **E**nable **C**o**MB** filter output Reg: 08 Bit: 4 Fu: SC
A chroma subcarrier reference output can be made available. At the same time the DC level at pin 30 switches from low to high.
0 = No subcarrier output at pin 30, DC voltage 0.1V, combfilter off
1 = Subcarrier output at pin 30, DC voltage 4.2V, combfilter on
(for non-comb filter applications this bit and pin can also be used as universal DC-control pin)

HBC : **H**elper **B**lanking **C**onditional Reg: 01 Bit: 5 Fu: SC
If set = 1 the helper blanking depends on the state of the **SNR** bit.

HOB : **H**elper **O**utput **B**lanking Reg: 01 Bit: 6 Fu: SC
Blanking of the YUV outputs during PALplus or EDTV-2 helper lines.

This mode is used to blank-out the helper chrominance signals in the luminance and chrominance path when a PALplus/EDTV-2 input signal is applied, but no helper demodulation is wanted, for instance when the signal conditions are not good enough. The helper blanking can only be activated when a norm signal is detected, indicated by output bit **NRM = 1**. During line scan the black level is filled in.
For PALplus (50Hz, 625 lines) the blanking is active on lines 275 - 371 and 587 - 59.
For EDTV-2 (system M, 60Hz, 525 lines) the blanking is active on lines 230 - 312 and 493 - 49.

Helper blanking as function of **HOB, HBC** and **SNR** bits:

HOB	HBC	SNR	helper blanking
0	X	X	off
1	0	X	on
1	1	0	off
1	1	1	on

HD : **H**elper **D**emodulation Reg: 01 Bit: 4 Fu: SC
0 = off
1 = on, PALplus mode

At **HD = 1** and in combination with output bit **NRM = 1**, demodulation of PALplus helper lines is possible during lines 24-59, 275-310, 336-317 and 587-622. In this situation the YC comb inputs (if selected) are no longer used and the input selector switches to the active CVBS input. Also the **BPS** bit is forced to **1** (baseband delay line bypassed). A black set-up of 200mV is added to the complete luminance output signal including luminance scaling from 1.0Vbl-wh to 0.8Vbl-wh and an extra black set-up of 400mV during the helper lines is added to prevent clipping of the demodulated helper signal. The reference line 22 with the 200mV black set-up and 400mV helper set-up voltages is generated (see also page 41, Fig 11).

XD..XA : **X**-tal definition Reg: 00 Bit: 1,0 Fu: SU
Indication which Xtals are connected to the oscillator pins: The Xtal oscillator frequency is used to calibrate the horizontal frequency. Therefore the software must indicate which Xtals are connected, before calibration takes place. Validity of the I²C transmission should be verified via status byte 01_{HEX}, bits **SXA** , **SXB**, **SXC**, **SXD**. These bits should be identical to the values of **XA**, **XB**, **XC**, **XD** that were written.

XA,XB,XC,XD	CONDITION
0	Xtal not present
1	Xtal present

Output control bits:

CD3..CD0 : **C**olour **D**etection Reg: 00 Bits: 3,2,1,0 Fu: SC
Reflects the colour standard that is identified by the TDA9321 H

CD3	CD2	CD1	CD0	Colour standard	used Xtal
0	0	0	0	no colour standard identified	A/B/C/D
0	0	0	1	NTSC	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	B
0	1	0	0	PAL	B
0	1	0	1	NTSC	C
0	1	1	0	PAL	C
0	1	1	1	NTSC	D
1	0	0	0	PAL	D
1	0	0	1	SECAM	A
1	0	1	0	illegal forced mode	

SXD..SXA : **S**tatus of **X**tal indication Reg: 01 Bit: 0,1,2,3 Fu: SU
This reflects the selection made by **XD**, **XC**, **XB**, **XA** so that software can verify validity of the I²C transmission.

SXD, SXC, SXB, SXA	Condition
0	no Xtal connected
1	Xtal connected

Analogue control:

HUE : **HUE** Reg: 03 Bit: 5..0 Fu: UC
The hue control is active when the NTSC colour system is received and also when PALplus helper lines are demodulated (**HD = 1**).
Nr. of steps: 63
Range: -40 .. +40 degrees

2.2.5.7 Power and protection.

Output control bits:

POR : **P**ower **O**n **R**eset Reg: 00 Bit: 7 Fu: SC
Power on reset: Indicates detection of a power failure (including power down during stand-by or switch-off of the TV set). It remains high until the status bytes have been read successfully to enable also to detect short power failures. When a failure is detected, the internal data is not reliable any more and should be refreshed. During normal operation the POR status should be read continuously, before sending any input data. During start-up, the IC status should be read until the POR bit is low, immediately followed by the start-up procedure (see chapter 2.2.5 .)

0 = Device operational
1 = Power failure detected

2.2.5.8 Device select.

Output control bit:

ID3..ID0 : Device **ID**entification code Reg: 03 Bit: 7..4 Fu: SC
This can be used to verify which IC type is connected.

ID3	ID2	ID1	ID0	Type number	Comment
0	0	0	1	TDA9321 H	Full multi system video input processor with QSS
				Spare	All other ID3..0 combinations, for future extensions

3. APPLICATION INFORMATION

3.1 General

In section 2 device information has been given. This section describes the application aspects of the pins.
The component choice often is a compromise and depends on the requirements defined by the customer.
By means of this section one is able to decide whether components can be changed and what the consequences will be.
Please refer to page 103 for a complete application diagram of TDA9321 H.

3.2 Application remarks per functional block and per pin

The pins will be described per functional block analogue to section 2. The pin voltage may not exceed Vcc+Vbe.

3.2.1 Vision IF & sound IF

*** IF input, pin 2,3**

The PLL frequency range is 32-60MHz.
The IF input impedance is 2kΩ in parallel with 3pF and matches the required load for commonly used SAW filters. A DC coupling is allowed, so no series capacitors between SAW filter and IF input are necessary. For maximum IF-stability it is advised to make the signal path from tuner to IF-input as symmetrical and close as possible.

*** IF VCO tuned circuit, pin 7,8**

The IF VCO tuned circuit is applied to these pins. The resonance frequency is two times the IF-frequency and in a range of 64-120MHz. This range is suitable for the IF standards as 33.4, 38.9, 45.75 and 58.75MHz.
The VCO frequency can be adjusted by I²C bus so a fixed coil can be used. The figure below gives the VCO input circuit. The data given in the table is useful to determine the VCO tuned circuit.

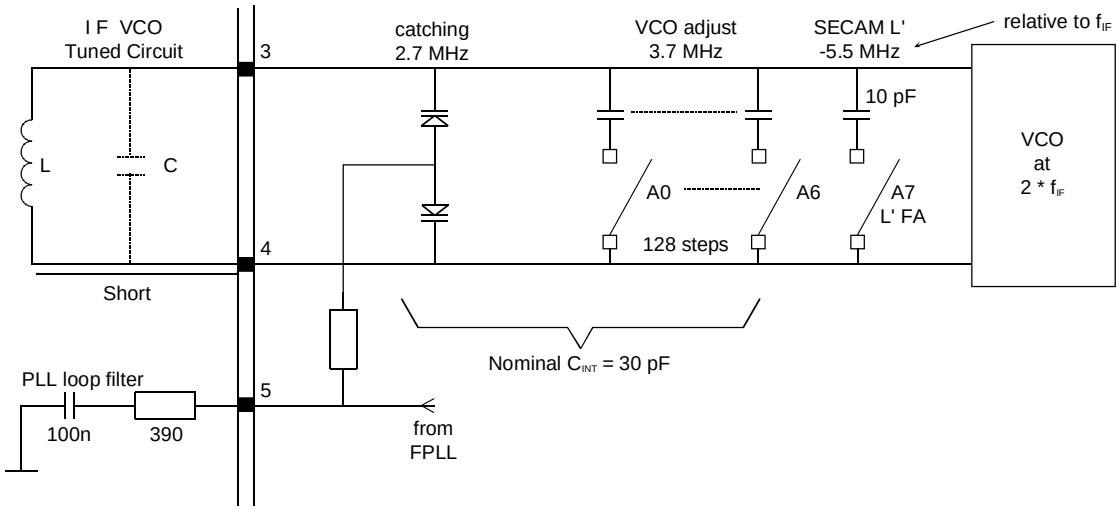


Fig 12 : IF-VCO input circuit

1 Coil data:

IF-input frequency, f_{IF}	38.9	45.75	58.75	MHz (32-60MHz)
VCO frequency, $f_{vco}=2*f_{IF}$	77.8	91.5	117.5	MHz (64-120MHz)
L (very short at pin)	140	100	61	nH
Cint typical	30	30	30	pF
$L*C_{int}$	4185	3025	1835	nH*pF (for f_{vco})
Q0 (unloaded)	>60	>60	>60	>60
Turns for coil per slot	S=4	S=3/4,T=1, U=1 3/4	S=T=U=1	Toko core, 5KM

Table 9 : IF-VCO tuned circuit data

Remarks:
1: The coil data given in the table are approximated values. The exact value must be evaluated per application
Only a coil is required between pin 7 and 8. Thus without external capacitor C.
Short connection of the coil to these pins is required in order to minimise both parasitic capacitance and series inductance (inductance is approx. 10nH/cm).
2: The internal capacitance, C_{int} typical = 30pF for: nominal f_{IF} , A0-A6 set to typical 63 and L'FA=0
3: L*Cint has been calculated for different fvco for easy determination of the LC values. The resonance frequency fvco= 1/ (2*π*√L*(C+Cint)). Example for 38.9MHz: 4185/30pF=140nH

The figure below gives the relation between the internal VCO capacitors versus the IF-frequency as given in the previous table.

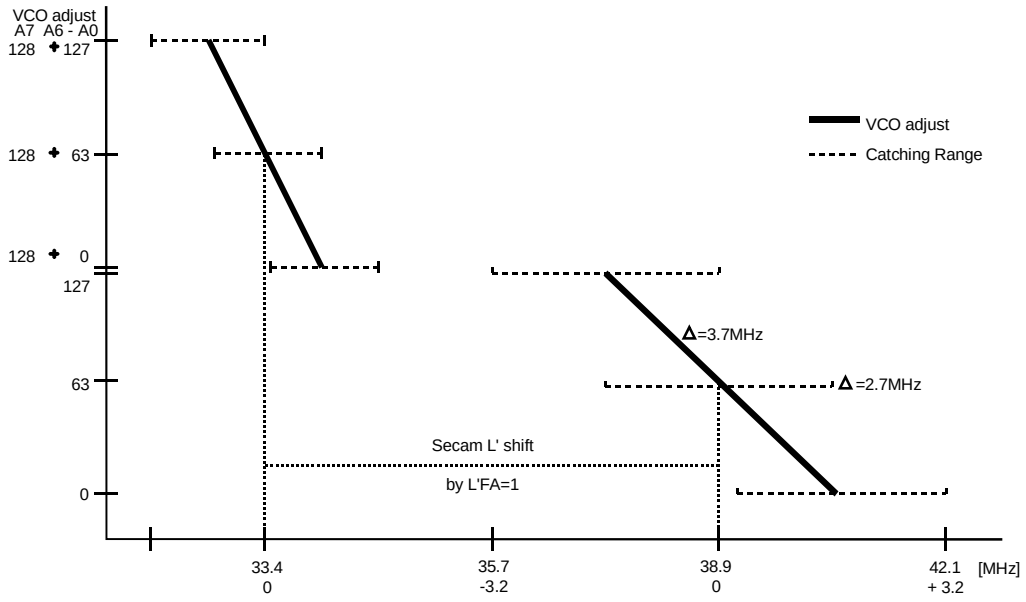


Fig 13 : Relation ship VCO-capacitors versus VCO-frequency

The VCO frequency is adjustable via the I²C bus bits A0-A6, (3.7MHz in 128 steps). See also section Alignment.
For the SECAM L' mode (with L'FA=1, bit A7), the frequency is shifted -5.5MHz typical. The PLL catching range (2MHz) is determined by the internal varicaps and the PLL-loopfilter control voltage.

2 SECAM L' application:

For SECAM L' applications the picture carrier frequency must be shifted from 38.9MHz to 33.4 or either 33.9MHz, depending on the type of SAW filter. The frequency step then is -5.5 or -5MHz (relative to 38.9MHz only). With previous concepts a lot of external components were required to achieve this frequency step. With the TDA9321 H this function can be realised very easy by means of I²C bus bit A7; L'FA. When L'FA=1 a capacitor of 10pF is added to the VCO tuned circuit. The frequency therefore changes with -5.5MHz typical.
A smaller frequency change of -5MHz can be realised when a small external capacitor is added across the VCO coil. The table below gives data for both 33.4 and 33.9MHz standards.

IF-input frequency, fIF	33.4	38.9	33.9	38.9	MHz (32-60MHz)
VCO frequency, fvco=2*fIF	66.8	77.8	67.8	77.8	MHz (64-120MHz)
Switching of internal 10pF	L'FA=1	L'FA=0	L'FA=1	L'FA=0	
L (very short at pin)	140	140	132	132	nH
C (only for 33.9MHz)	0	0	1.6	1.6	pF
Cint typical	30+10	30	30+10	30	pF
L*(C+Cint) 5676	5676	4185	5510	4185	nH*pF (for fvco)
Q0 (unloaded)	>60	>60	>60		
Turns for coil	S=4	S=4	S=4	S=4	Toko core, 5KM

Table 10 : IF-VCO tuned circuit data for SECAM-L'

By adding an external capacitor of aprox. 1.6pF (see calculation below) the total capacitance at the IF-VCO input is increased from 30 to 31.6pF. In this condition the influence of the 10pF capacitor is relatively less than compared to 30pF. Consequently the frequency step will be smaller, thus not -5.5MHz, but -5MHz instead.

Both C and L can be calculated by means of two equations used in the table above:

(30pF+ 0pF+C)* L = 4185
(30pF+10pF+C)* L = 5510 => C =(4185(30+10)-5510*30) /(5510-4185) =1.6pF and
L = 4185/(30+1.6)= 132nH

Remark: these figures are approximated values and must be evaluated per application.

For SECAM L' a commonly used IF-frequency is 33.9MHz. Sometimes the IF frequency is adjusted slightly above 33.9MHz in order to achieve a best compromise between low colour carrier suppression and good sound rejection. Important is also that the picture carrier suppression (at second Nyquist slope) is 6dB. Such adjustment is suitable for both quasi split sound and intercarrier sound.

3 Catching/holding range of IF-PLL:

Once the IF-PLL is in-lock, and thus within the catching range, the VCO automatically tracks to the incoming IF- frequency. Fig 14 gives the PLL-loopfilter (pin 6) voltage versus the IF-frequency. The loopfilter voltage swing is limited by an upper and lower clamp. The PLL-catching range is determined by both voltage swing (1.4V) and variation of the internal varicaps (+/-1.5pF).
The AFC information is derived from this loopfilter voltage and placed in the middle of the holding range.

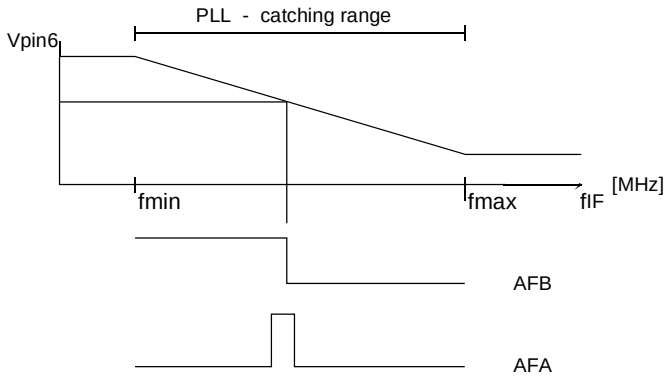


Fig 14 : PLL-loopfilter versus IF-frequency

4 Determination of IF-VCO coil value:

The IF-VCO coil values given in the table are approximated values. The optimal value must be evaluated per application. Important variables are: parasitic capacitance between pin 7 and 8 and series inductance. Both are dependent upon the PCB layout.
Following procedure have to be carried out during TV-set development:

- Mount TDA9321 H sample in a final PCB.
  Use a plastic sample (no ceramic since the capacitance is bigger then)
  Don't use an IC socket since this increases the parasitic capacitance.
- Set VCO adjust, bits A0-A6 to 63 (middle of range)
- Apply a 38.9MHz (or other standard frequency) signal to the IF-input
- Align the VCO-coil between pins 7 and 8 by manual adjust for correct AFC information.
  The VCO adjustment is correct when the AFA bit is "1" and the AFB bit is altering.
- Take out the VCO-coil and measure the inductance
- This coil value can be ordered by your supplier, (further coil specifications see next)

5 Coil specification:

- Tolerance < 2% in order to ensure catching of the IF-PLL
- Temperature coefficient as small as possible. TOKO specifies approx. +100ppm/K with coils given below.
  For both coil and IC has been measured at 38.9MHz: -260kHz/70deg = -3.7kHz/K. The frequency variation therefore becomes -95ppm/K, an equivalent inductance variation becomes +190ppm/K.
- Q factor >60 (unloaded)
- no build-in capacitor
- windings in lowest slots for optimal EMC behaviour.

Evaluation samples from TOKO are:

IF frequency [MHz]	VCO frequency [MHz]	Coil [nH]	TOKO Sample number
38.9	77.8	150	P369INAS-159HM
45.75	91.5	100	P369INAS-160HM
58.75	117.5	70	P369INAS-161HM
Temperature Coefficient			30+/- 100ppm/°C

Table 11 : IF-VCO coil types

In order to meet these specifications following considerations have been taken.

- A tolerance of less than 2% seems to be possible only for pre-adjusted coils. The increase of costs for pre-adjustment is being neutralized because no build-in capacitor is needed.
  The 5KM adjustable coil from TOKO is recommended.
- The coil temperature coefficient has been minimised by removing the ferrite pot core. The only ferrite that remains is for adjustment. Ferrite material: 80-120MHz.
  The Q-factor now is less but still >60, which is suitable for the IF-PLL.
- Normally the coil windings are placed in the highest slots, beneath the pot core. Because the pot core has been removed it became possible to place the windings in the lowest slots.
  This improves the EMC behaviour since the coil wire length then is minimal for parasitic cross talk.

*** Video output, pin 10**

The video output signals are:

	B/G	L	
Video amplitude is typical	2.5	2,5	[V]
top sync (fixed by AGC)	2	-	[V]
top white (fixed by AGC)	-	4.5	[V]

The sound carrier level will be suppressed by the SAW filter in QSS applications.

Although the video output impedance is low it is recommended to avoid high frequency current in the output due to for instance sound trap filters. This can be achieved by means of an emitter follower at the video output with a 1kΩ resistor in series with the base.

The sound trap filters are optional. The need for it depends on the TV systems used and SAW filter selection.

Cross talk INT->EXT aspects:
- Avoid layout tracks with video signals being close to the AV input
- Decouple collector of emitter follower at pin 10 or avoid too much current in the emitter follower.
- At no antenna signal condition the video noise peak-peak level is higher than the normal video amplitude. Depending upon application this might give extra cross talk and line jitter. This noise level can be reduced by means of I²C bus **IFS**=1. This reduces the IF-gain by 20dB. In practice overall sensitivity reduction will only be 12dB due to the tuner noise.

Switch-off IF part:
- See Application of non-used pins at page 85.
- Switch off the IF-part by means of I²C bus command **VSW**=1 ; for minimal power consumption have also **IFO**=1
  In this condition the video output pin voltage is 0V and tuner AGC output is forced low for minimal tuner gain.
- CVBS input pin 14 can be used as extra input pin; have **VSW**=1 to ensure correct functioning of **IFI.**
  Make **VIM**=1, optional is **VID**=1

*** Groupdelay input, pin 12**

The required input amplitude is 2Vpp. This signal is derived from the IF-video output signal pin 10, via the sound trap filters.
The coupling capacitor is 47nF. The maximum source impedance is not critical but recommended to be less than 1k.

*** Groupdelay output, pin 13**

The output amplitude is 2Vpp, and direct related to the input pin 12. The signal must be fet to an emitterfollower plus divider in order to get 1Vpp at the CVBSint input pin 14.
De groupdelay for system BG can be switched on/off via I2C command GD. The groupdelay characteristic is given in the device specification.

*** AFC output I²C bus: AFA, AFB**

The AFC output is available by I²C bus and is used for VCO adjustment and feedback signal to the tuner. The VCO needs to be adjust only once in the TV production line.

The digital AFC signals AFA and AFB are derived from the PLL-loopfilter pin 6. The figure below gives the bit status in relation with the incoming IF-frequency and VCO-adjust setting.

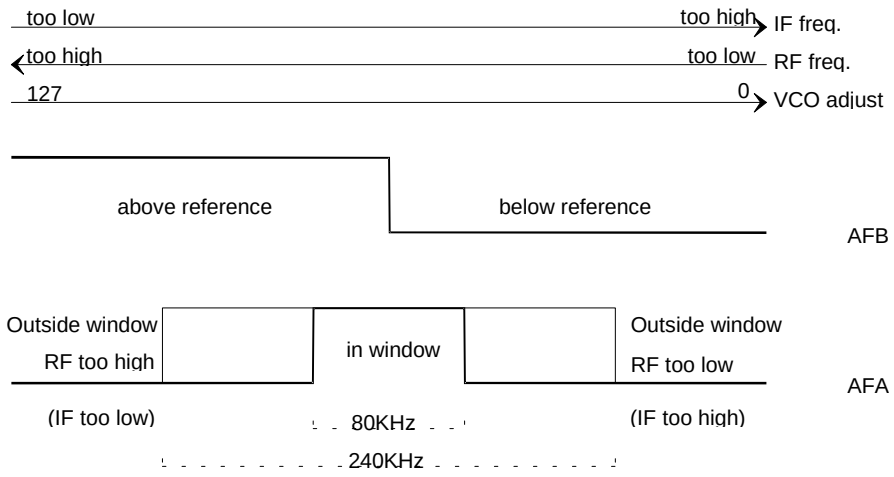


Fig 15 : AFC output bits

The VCO is correct adjusted when the AFA bit is "1" and the AFB bit is altering.

Remarks

- The AFC information is only valid when the IF-PLL is in-lock, thus **PL**=1.
- **PL**=1 can also be caused by a sound carrier. To make sure a video signal is recognized it's advised to check in addition: video ident (**IFI**) or coincidence detector (**SL**).
- The width of the "in-window" bit AFA can be increased from 80-> 240kHz by means of **AFW**=1 . This allows bigger frequency steps in order to speed-up the search tuning.

*** PLL loopfilter, pin 6**

Standard loopfilter is: R=390Ω and C=100nF in series to ground. The loopfilter bandwidth is 60kHz and is optimal for both fast catching and sufficient video suppression for optimal sound performance.

The loopfilter time constant can be changed by I2C bus function **FFI** (Fast filter IF-PLL)
When **FFI**=1, the PLL can better handle non-standard transmitter signals with large phase modulation.
The standard PLL loopfilter value can be left unchanged.

FFI=0 Normally selected for standard transmitter signals
FFI=1 Specially to handle non-standard transmitter signals with large phase modulation.
The function can be used for both positive and negative modulated signals.

When to program **FFI**=1:
- during initialisation and for TV stets for special market areas only
(in our previous concepts the loopfilter value had to be increased for those market areas)
- via service mode in case of specific field problems while **FFI**=0

*** AGC decoupling capacitor, pin 4**

Positive/ negative modulation
The optimal AGC capacitor value is 2.2µF and has been defined for an optimal compromise between AGC speed and line tilt for all AGC modes (both negative/positive modulation).
For maximum stability the AGC capacitor must have a short connection to ground.

Negative modulation only:
For applications with negative modulation only it is allowed to increase the AGC speed by lowering the capacitor value. This e.g. to improve airplane flutter performance. The minimum value is determined by acceptable line tilt and weak signal catching. To our experiences the value should be greater than 330nF. First evaluate a minimal capacitor value for RF levels such the tuner AGC is not active. This to eliminate a second AGC loop via the tuner.

Leakage:
The allowable leakage current: < 10µA for negative modulation and
< 200nA for positive modulation.
It is not recommended to have any external resistor to +8V or ground. This reduces the AGC performance considerably for weak signal conditions.

AGC actions:
Optimal IF performance is achieved via gating functions, derived from the horizontal oscillator. They become automatically active once the coincidence detector SL=1. In external mode the top white AGC remains available as this function does not need a gating signals from the horizontal oscillator.

AGC in INT. mode	AGC in EXT. mode	
top white AGC	top white AGC	
black clamp AGC *)	-	
AGC line gating *)	-	*) activated when **SL**=1

Maximum AGC performance is achieved in internal mode and when **SL**=1. This independent upon the video ident mode **VIM**.

*** Tuner AGC output, pin 62**

This output is used to control (reduce) the tuner gain for strong RF signals.
The tuner AGC is an open collector output which is acting as a variable current source to ground.
The external pull-up resistor determines the steepness of the tuner output voltage swing and therefore the maximum IF-input amplitude variation, called slip. Once the tuner AGC is active the IF input signal level is constant within the slip.
The level on which the tuner becomes active (Tuner take over point) can be adjusted by I²C bus.
With a pull-up resistor of t.b.f. kΩ the slip is 2 dB typical.

In this application the time constant of the tuner AGC can be defined separately from the gain (pull-up resistor) setting. Stability of the loop becomes difficult when the loopgain is too high (pull-up resistor >>10kΩ). Special attention on stability is required for reception of positive modulated signals.

Normally the output application circuit is designed for an output current swing of 1-2mA. In order to improve the dynamic behaviour during channel switching it is possible to sink with a current of minimal 5mA (8mA typical). The max voltage is Vcc+1V.

Notice that when the IF-part is muted via **VSW**=1, than the tuner output pin is grounded for minimum tuner gain.

*** Tuner take over adjust, I²C bus: Tuner take over**
See section 4, ALIGNMENTS at page 87.

*** SIF input, pin 63,64**

The SIF input impedance is 2kΩ in parallel with 3pF and matches the required load for commonly used SAW filters. A DC coupling is allowed, so no series capacitors between SAW filter and IF input are necessary. For maximum IF-stability it is advised to make the signal path from tuner to SIF-input as symmetrical and close as possible.

*** QSS/AM output, pin 5**

This pin is a combined output pin. The signals can be split-up via an external filter, see below.
The output impedance is 250E, the DC level is 3.3V

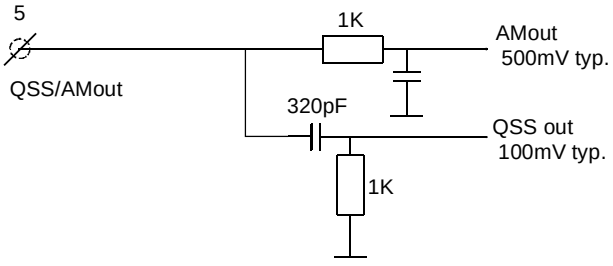


Fig 16 : Filters to separate QSS/AM signals

BTSC application:
The bandwidth is 100kHz minimal, which makes the output also suitable for the USA BTSC stereo system. For more info on BTSC stereo, see also report TDA837X-N2, AN96070, page 28.

*** SIF-AGC, pin 1**

The optimal AGC capacitor value is 2.2µF and has been defined for an optimal compromise between AGC speed and AM frequency behaviour. A smaller capacitor value for AM sound will increase the low corner frequency (the harmonic distortion will not be effected as the AGC is an average detector)
The AGC time constant is automatically adapted for positive and negative modulation. For negative modulation the AGC is made a factor 10 faster. For maximum stability the AGC capacitor must have a short connection to ground.

*** Switched outputs, pin 19,22**

The two I^2C bus controlled (OS0, OS1) output ports which can be used to switch sound traps, SAW filters or other external components. Output level is 0.1V - 5V typ. The sink/source current 2mA.

3.2.2 Horizontal and vertical synchronization

*** PHI-1 control loop, pin 58**

The loopfilter connected to pin 43 is suitable for various signal conditions as strong/weak and VCR signal. This is achieved by switching of the loopfilter time constant by changing the PHI-1 output current. Via I²C bus **FOA/B**, different time constants can be chosen, including an automatic mode which gives optimal performance under varying conditions.
Most common is used:

FOA/B = 0 0 (automatic mode) for off air signals
FOA/B = 1 1 (fast mode) for external inputs, optimal VCR performance

See chapter device description, horizontal and vertical synchronisation for more details.
To avoid disturbances in the loop, the filter should be connected to the ground pin as closely as possible.
The recommended values for the loop filter are:
C = 4n7, R = 15 kOhm, C = 1µF.
When under special conditions fast loop reaction is required, the advised limit values are:
C = 2n2, R = 18 kOhm (max. 22 kOhm), C = 1µF.

The PHI-1 loop can be switched off by the I²C bus function **POC**. When **POC** = 1, a valid incoming signal can only be detected reading **IFI** (**SL** is always 0 when **POC** = 1). **IFI** should be connected to the selected video source for this purpose. It is of course also possible to use an external ident circuit.

When **VID** = 0, **IFI** controls the PHI-1 time constant switching between normal (**IFI** = 1, valid signal detected), and very slow (**IFI** = 0, no valid signal detected). In this way, stable OSD is obtained when no signal is present. This mode is very handy for search tuning.

VCR performance must be checked in the fast PHI-1 mode; **FOA/FOB** = 1 1.
VCR head jump tests (with 16µs phase jumps) must be tested with these jumps during vertical retrace and not during vertical scan. The sync processing includes special features as increased PHI-1 current during vertical retrace that ensures fast settling.

*** Sandcastle output pin 59**

This output pin delivers a two level sandcastle which pulses are internally derived from the horizontal oscillator:

- The normal level is $\leq$ 1 Volt (0.5 Volt typical)
- During horizontal and vertical blanking the level is 2.5 ± 0.3 Volt
- During clamp pulse / burstkey the level is $\geq$ 4.2 Volt (4.5 volt typical)

The horizontal blanking lasts 10 µs and the trailing edge starts 3.2 µs before the middle of the sync of the selected CVBS/YC signal.
The clamp/burstkey pulse has a width of 3.6 µs and starts 6.4 µs after the trailing edge of the horizontal blanking
The vertical blanking starts line 310.5 / 623 and lasts 26 lines for 50 Hz and starts line 263 / 525.5 and lasts 22 lines for 60 Hz signals.
The sandcastle output can sink and source 0.7 mA which implies the use of a buffer when long tracks and/or many other IC's are connected to the sandcastle.
For the timing relation between CVBS/YC, H_A/CLP and V_A, see the figure further in this chapter.

*** Horizontal in/output, pin 60**

This pin can be configured as ouput or input, pending on bit **ECL**.

For **ECL** = 0, the circuit switches to internal clamp mode and the internal H_A/CLP pulse is provided at the output. The choice between H_A and CLP is made with the bit **HO**, 0 = CLP pulse, 1 = H_A. Both pulses are positive.
The H_A pulse has the same timing as the sync pulse of the selected CVBS/YC signal but with a delay of 0.45 µs, due to the low pass filtering at the sync input.
The CLP pulse has the same timing as the clamp/burskey pulse of the sandcastle.
The output is a push-pull configuration with the following specification:

V_{OUT} high $\geq$ 4 Volt
V_{OUT} low $\leq$ 0,4 Volt
$I_{SINK/SOURCE}$ $\geq$ 2 mA.

After power-up, the H_A/CLP pulses are suppressed until **POR** = 0, all I^2C registers are written and calibration of the horizontal oscillator is completed.
For the timing relation between CVBS/YC, H_A/CLP and V_A, see Fig 18 at page 74.

For **ECL** = 1, the circuit switches to external clamp mode and pin 60 becomes input. The input specification is:

V_{IN} high $\geq$ 2.4 Volt
V_{IN} low $\leq$ 0.6 Volt
Input impedance $\geq$ 3 Mohm

The timing of the external clamp pulse with respect of the related YUV/RGB signals should be similar to the timing of the internal CLP pulse.
The external clamp pulse should have positive polarity and have a minimal pulse width of 1.8 µs, preferred value is 3.6 µs.
Note that in external mode also the vertical pulse V_A is suppressed and therefore has to be provided externally!

*** Vertical output pin 61**

This output generates a positive vertical pulse V_A for vertical synchronisation.
The positive edge of V_A starts 37.7 µs after the first edge of the vertical synchronisation of the composite sync signal. The positive edge is positioned 32 µs before the first following positive edge of the CLP pulse (odd fields) or coïncides with the positive edge of the CLP pulse (even fields).
The duration is 160 µs (2.5 lines) for 50 Hz signals and 192 µs (3 lines) for 60 Hz signals.
The output has the same specification as pin 60 horizontal output:

V_{OUT} high $\geq$ 4 Volt
V_{OUT} low $\leq$ 0,4 Volt
$I_{SINK/SOURCE}$ $\geq$ 2 mA.

Note that V_A is suppressed when pin 60 is configured as input for an external clamp pulse (**ECL** = 1).
For the timing relation between CVBS/YC, H_A/CLP and V_A, see Fig 18 at page 74.

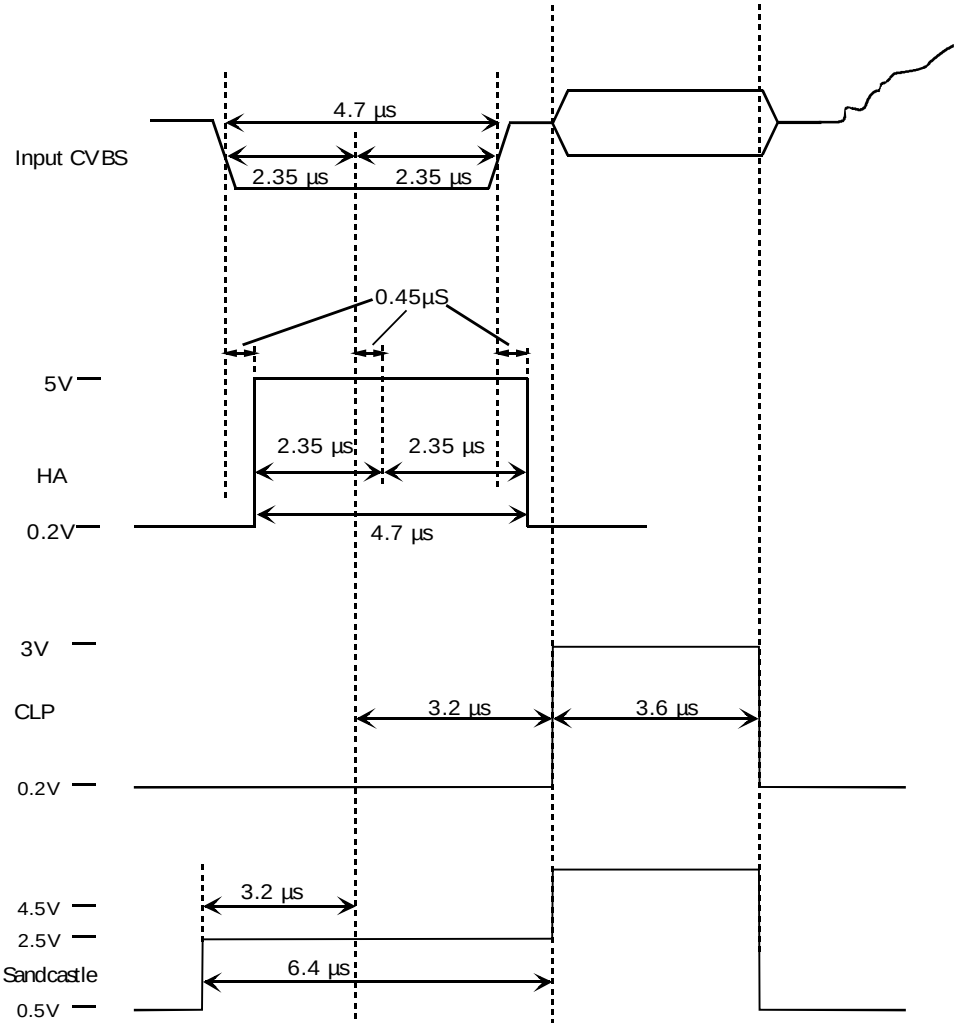


Fig 17 : Horizontal timing H_A/CLP pulse

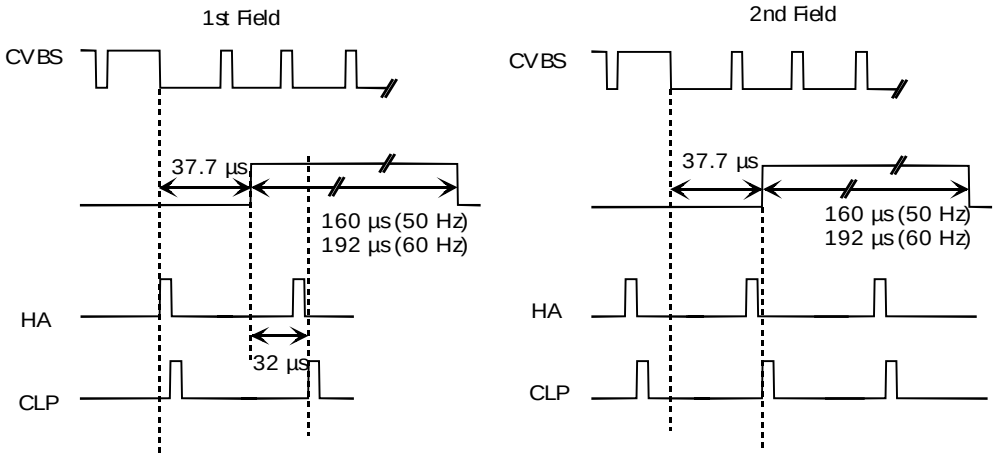


Fig 18 : Vertical timing H_A/CLP pulse

3.2.3 Filters and Switches,

*** $CVBS_{INT}$ input** **pin 14**

It is recommended that the CVBS input amplitude is 1Vpp (inclusive sync amplitude). This, because the noise detector switches the phi1 loop to slow mode (i.e. auto phi1 mode when **FOA, FOB** = 0, 0) when noise level exceeds 100mVrms (i.e. at S/N of 20dB).
Example:

When the attenuation between the IF video output and $CVBS_{INT}$ input is such that the video amplitude is less than 1Vpp, then the noise detector becomes active at a lower RF level. This causes line phase jitter for low RF signals since the noise detector is not switched at the optimal S/N ratio of 20dB.

For reduction of $CVBS_{INT}$ at group delay output pin 13 to 1V, the application of Fig 19 can be used.
The 2Vpp output can be used for scart application.

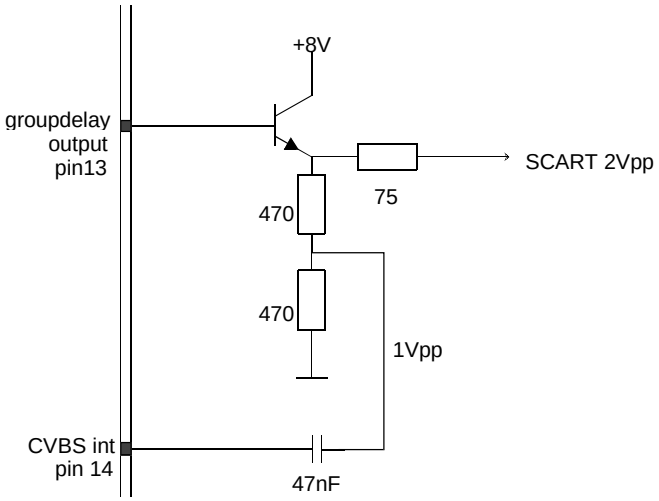


Fig 19 : $CVBS_{INT}$ signal reduction to 1V at group delay output.

$CVBS_{INT}$ source impedance:
The sync separator sensitivity is optimal when the source impedance, R_{SOURCE}, is low; this is important for compressed sync performance. During top sync, clamping action occurs where the clamp current is 100uA. The sync is reduced by R_{SOURCE} * 100uA implying less sync separator sensitivity for greater source impedance.
If a large source impedance (>500•) exists in the application then it is advised to apply an extra buffer in order to achieve optimum sync separator performance.
The chosen coupling capacitor is a compromise between fast clamping action and minimum CVBS line sag. With a clamping current during top-sync of 100uA and an input current outside top-sync of 4uA, then the recommended coupling capacitor is minimal 47nF.

*** CVBS1, CVBS2, CVBS/Y3, CVBS/Y4, COMBY inputs** **pins 16, 18, 20, 23, 28**

It is recommended that the CVBS or Y input amplitudes are 1Vpp (inclusive sync amplitude). This, because the noise detector switches the phi1 loop to slow mode (i.e. auto phi1 mode when **FOA, FOB** = 0, 0) when noise level exceeds 100mVrms (i.e. at S/N of 20dB).
The input signal is AC coupled to pins 16, 18, 20, 23, 28. During top sync, clamping action occurs where the clamp current is 100uA. The coupling capacitors that are chosen are a compromise between fast clamping action and minimum line sag. With a clamping current during top sync of 100uA and an input current outside top-sync of 4uA, then the recommended AC coupling capacitors are minimal 47nF.
If a large source impedance (>500 •) exists in the application then it is advised to apply an extra buffer (Fig 20) in order to achieve optimum sync separator performance.

*** Chroma inputs** **pins 21, 24, 29**

The supplied chroma input burst amplitude should be nominally 300mVpp (assumed is a colour bar signal with 75% saturation and with chroma/burst ratio of 2.2:1). The chroma inputs are internally clamped to groundlevel via 100K. The external AC coupling capacitor with 100K forms a high pass filter.
A recommended coupling capacitor is 1nF; the high pass filter cut off frequency is then approximately 2KHz.

*** COMBCVBS output** **pin 26**

The output amplitude is 1Vpp (transfer gain ratio between CVBS inputs and this output is 1). The maximum output impedance is 250 •. For application with the SAA4961 combfilter it is advised to use an emitter follower circuit as shown in Fig 20.
It is advised that the signal paths to the comb filter and back to the TDA9321 H are as short as possible so as to avoid crosstalk from interference sources. The follower is placed as close as possible to the output pin.

*** $CVBSO_{PIP}$** **pin 32**

The output amplitude is 1Vpp (transfer gain ratio between CVBS inputs and this output is 1). The maximum output impedance is 250 •. For application it is advised to use an emitter follower circuit as shown in Fig 20.
It is advised that the signal path to the following circuit is short so as to avoid crosstalk from interference sources. The follower is placed as close as possible to the output pin.

*** $CVBSO_{TXT}$,** **pin 34**

The output amplitude is 2Vpp (transfer gain ratio between CVBS inputs and this output is 2). The maximum output impedance is 250 •. Because of the 2Vpp output amplitude this output is also suitable for scart application. For application it is advised to use an emitter follower circuit as shown in Fig 20.
It is advised that the signal path to the following circuit is short so as to avoid crosstalk from interference sources. The follower is placed as close as possible to the output pin.

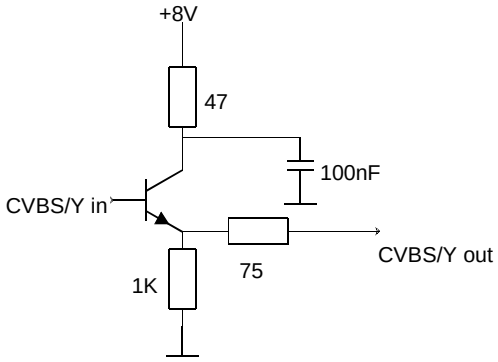


Fig 20 : CVBS buffer

*** AV1, AV2 inputs** **pins 15, 17**

Via these inputs it is possible to sense 3 voltage levels on each pin and read out this info via I2C bus bits **S1A, S1B** and **S2A, S2B**. Internal switching levels of the voltage comparators are typical 2.2V and 5.5V, input resistance is 100K.
For detection of the status of pin 8 of a SCART connector it is necessary to use a voltage divider with a ratio of 2/3 between the SCART connector and pin 15 or 17. This for matching the different levels of the SCART norm and the AV1, AV2 inputs. This voltage divider should have an impedance of max. 10K.
See also page 30: *** CVBS, Y/C signal selection.**

*** RI1, GI1, BI1 inputs** **pins 36, 37, 38**

The RGB input signals (nominal signal amplitude of 700mVpp) are AC coupled to pins 36, 37 and 38 respectively. When using as YUV inputs then the signal amplitudes must be 1000mVpp, 1300mVpp and 1050mVpp respectively. These YUV signals are connected to pins 37, 38 and 36 respectively. Clamping action occurs during burstkey period. The coupling capacitors chosen are a compromise between fast clamping action and minimum line sag. Capacitors of 22nF or greater can be used
The source impedance of the RGB signals should be kept as low as possible (< 500•) for correct clamping operation.

*** RI2, GI2, BI2 inputs** **pins 41, 42, 43**

The RGB input signals (nominal signal amplitude of 700mVpp) are AC coupled to pins 41, 42 and 43 respectively. Clamping action occurs during burstkey period. The coupling capacitors chosen are a compromise between fast clamping action and minimum line sag. Capacitors of 22nF or greater can be used
The source impedance of the RGB signals should be kept as low as possible (< 500•) for correct clamping operation.

*** RGBIN1, RGBIN2** **pins 39, 40**

YUV internal is selected if the voltage at pins 39 or 40 is lower than 0.4V and is independent of the status of the I2C control bits **IE1** and **IE2**. For RGB/YUV insertion the voltage on the pins 39 and/or 40 must have a value between 0.9V and 3.5V and also the **IE1** and/or **IE2** bits must be 1 in this case.
RGBIN2 insertion has priority above RGBIN1, i.e. it is possible to insert a PIP signal via RGB2 inputs within the signal supplied via RGB1 inputs. With the I2C output control bits **IN1** and **IN2** it is possible to sense the voltages on the RGB insertion switch input pins 39 and 40 continiously even if the I2C bits **IEI** and **IE2** are disabled.
Due to a max. input current of 0.2mA coming out of the insertion switch it is recommended to have a low source impedance (< 500•) at pins 39 and 40.

*** Y output** **pin 49**

The luminance output signal is approximately 1Vbl-wh with maximum output impedance of 250•. The black level is approx. 3.0V. In PALplus or MACP mode a black set-up of 200mV is added to the complete Yout signal including luminance scaling from 1Vbl-wh to 0.8Vbl-wh. This set-up/scaling prevents distortion of the chrominance component in the Yout signal, when supplying this signal to the external ADC's used in a complete PALplus concept.

*** UV outputs** **pins 50, 51**

The colour difference output signals have respectively a nominal output level of $1.33V_{pp}$ and $1.05V_{pp}$ for a standard EBU colour bar (75% chroma saturation). The DC level is approx. 2.4V and the output impedance of pins 29 and 30 is max. 250• when a colour system is identified.
It is possible to insert picture improvement IC's between the TDA9321 H and the TDA933X H output processor. If these devices need smaller YUV input amplitudes, then voltage dividers at the YUV outputs of the TDA9321 H will be necessary for correct matching.

Colour decoder

*** Xtal pins** **pins 54, 55, 56, 57**

To ensure correct operation of:
- sync calibration internal circuits,
- colour processing internal circuits,
- communication to combfilter via pins 25,27,

The Xtals have to be connected as follows:

Pin 54: 4.433619MHz
Pin 55: 3.582056MHz (PALN)
Pin 56: 3.575611MHz (PALM)
Pin 57: 3.579545MHz (NTSCM)

When the 4.433619MHz Xtal is used then it always has to be connected to pin 54. For correct communication between TDA9321 H and combfilter via pins 25 and 27, then the Xtals must be connected as stated in the tables below. When no combfilter is used then the 3.58MHz Xtals can be used at any of the pins 55, 56 or 57. It is not allowed to connect a 3.58MHz Xtal at pin 54.
The I2C bus write commands **XA, XB, XC, XD** must be in agreement with the hardware application before calibration takes place as given in tables below:

XA	Pin 54, Xtal 4.433619MHz
0	not connected
1	connected

XB	Pin 55, Xtal 3.582056MHz
0	not connected
1	connected

XC	Pin 56, Xtal 3.575611MHz
0	not connected
1	connected

XD	Pin 57, Xtal 3.579545MHz
0	not connected
1	connected

Validity of the I2C bus transmission should be verified via status byte 01_{HEX} bits **SXA, SXB, SXC, SXD.** these should be identical to the **XA, XB, XC, XD** bits that have been written as indicated in tables above.

The VCXO design is insensitive to spurious and 3^{RD} harmonic oscillation and for this reason different Xtal varieties can be used in application.

Another important VCXO parameter is the VCXO holding range which is influenced by the the Xtal parameters given in Table 12 : Typical Xtal below; here Philips Xtals are used as reference to have an indication of holding range.
These Xtals are tuned to f_L with C_L = 20pF in their manufacturing process. The series load capacitance should be C_L = 18pF in application to account for parasitic capacitance on and off chip and therefore to realise a symmetric holding range.

SYSTEM	CODE	Xtal parameters			Application	
	9922 520 ..	f_L(± 30ppm) tuned with C_L = 20pF	C_M (± 15%)	C_O	C_L	VCXO holding range
PAL BG/D/K/I	.. 00481	4.433619MHz	20.5fF	5.5pF	18pF	1400Hz (± 700Hz)
PAL M	.. 00479	3.575611MHz	14.5fF	4.5pF	18pF	1200Hz (± 600Hz)
NTSC M	.. 00478	3.579545MHz	14.5fF	4.5pF	18pF	1200Hz (± 600Hz)
PAL N	.. 00477	3.582056MHz	14.5fF	4.5pF	18pF	1200Hz (± 600Hz)

Table 12 : Typical Xtal (Philips)

The minimum VCXO holding range requirement is ± 70ppm of the subcarrier burst frequency f_{BURST}.
For 4.4MHz & 3.6MHz systems, this implies a minimum VCXO holding range of ± 300Hz & ± 250Hz respectively. In order to guarantee a catching range of ± 300Hz on 4.43MHz the minimum motional capacitance of the Xtal must have a value of 13.2fF; this takes into account IC deviation and Xtal application (C_L tol. ± 2%, f_L tol. ± 30ppm).
In order to guarantee a catching range of ± 250Hz on 3.58MHz the minimum motional capacitance of the Xtal must have a value of 9fF; this takes into account IC deviation and Xtal application (C_L tol. ± 2%, f_L tol. ± 30ppm).
In Table 13 : New series Xtal below, alternate Philips Xtals that meet these minimum requirements for holding/catching range, can be used.

SYSTEM	CODE	Xtal parameters			Application	
	9922 520 ..	f_L(± 30ppm) tuned with C_L = 20pF	C_M (± 15%)	C_O	C_L	VCXO holding range
PAL BG/D/K/I	.. 08009	4.433619MHz	13.7fF	4.0pF	18pF	min. ± 300Hz
PAL M	.. 08006	3.575611MHz	10.0fF	3.5pF	18pF	min. ± 250Hz
NTSC M	.. 08007	3.579545MHz	10.0fF	3.5pF	18pF	min. ± 250Hz
PAL N	.. 08008	3.582056MHz	10.0fF	3.5pF	18pF	min. ± 250Hz

Table 13 : New series Xtal (Philips)

The maximum VCXO holding range requirement is ± 275ppm of the subcarrier burst frequency f_{BURST}.
For 4.43MHz & 3.6MHz systems, this implies a maximum VCXO holding range of ± 1200Hz & ± 980Hz respectively.
Xtals tuned at series resonance (without external series capacitor C_L) in their manufacturing process increase the VCXO holding range. It is advised not to exceed the maximum VCXO holding range indicated above, especially in 3 and 4 norma applications.
Therefore in PAL M, PAL N and NTSC applications it is recommended to apply Xtals that are tuned at low values of C_L in their manufacturing process (i.e. C_L from 16pF -> 25pF).

Parasitic capacitance as indicated by C_P in VCXO pin application (see Fig 21) causes assymmetry in the holding range.

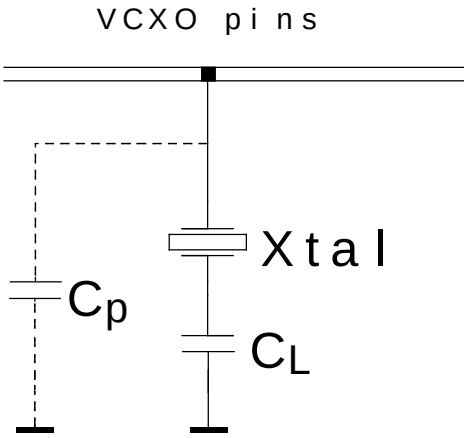


Fig 21 : VCXO pin application with parasitic capacitance C_P.

An indication of the influence of C_P on holding range symmetry is given in table below when using the reference Xtals of Table 12 : Typical Xtal :

SYSTEM	VCXO holding range		
	Normal Application	C_P = 1pF	C_P = 3.9pF
4.4MHz Xtal	+700Hz/-700Hz	+680Hz/-740Hz	+660Hz/-800Hz
3.6 MHz Xtal	+600Hz/-600Hz	+580Hz/-640Hz	+560Hz/-700Hz

It is advised to minimise parasitic capacitance C_P by:

- avoiding large ground planes around Xtal especially with double sided PCB,
- placing Xtal as close as possible to VCXO pin.

The maximal parasitic capacitance allowed on VCXO pins is 15pF.

*** Loop filter phase detector** **pin 52**

One of the important aspects of the PLL is the loop filter connected to pin 52; it influences the dynamic performance of the loop. The filter chosen gives an optimum transient response (see Fig 22). This ensures both an optimum for noise bandwidth and colour acquisition time.
Fast colour acquisition times are achieved since the phase detector is in high gain mode during non-acquisition.

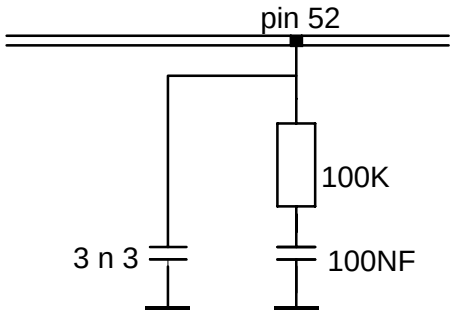


Fig 22 : PLL loop filter.

DC loading of phase detector pin must be avoided in application to prevent static phase errors.
For PCB layout considerations, it is advised that the loop filter circuit at pin 52 has a short return path to ground plane.

*** Subcarrier reference output (REFO)** **pin 30**

The reference output can be used as a reference for comb filter applications.
For PCB layout considerations, a short signal track connection with interface devices is advised. It is advised to minimise parasitic capacitance of pin to ground (i.e. avoid large ground planes around signal track).
The parasitic capacitance at this pin to ground should be less than 10pF.

*** COMBSYS1/SYS2 outputs** **pins 25, 27**

These outputs are used to inform the detected colour standard to the combfilter, the high output level is typ. 5V and the low level is typ. 0.1V.
The outputs can sink and source a current of 2mA.

*** SECAM PLLdecoupling (SECPLL)** **pin 53**

Variations in the SECAM PLL voltage during field scan, due to external leakage current, results in black level errors at the R-Y and B-Y outputs. Converted to input frequency a maximum error of 7kHz is permitted. The external voltage variations on the SECAM PLL decoupling capacitor should be below 2mV during field scan in order to meet these specifications. When using the recommended 100nF capacitor the max. leakage current must be kept below 10nA. A polyester metal film capacitor is a good choice here; the decoupling loop to ground must be kept small.

3.2.4 Supply, decoupling and grounding

*** Supply,** **pin 11, 45**

The TDA9321 H has two supply pins 11 and 45. Both pins must be supplied simultaneously (notice that the IC has not been designed to use one of both pins as start pin).
For optimal performance both pins need a separate decoupling.
The supply settling should not be faster than 10ms.

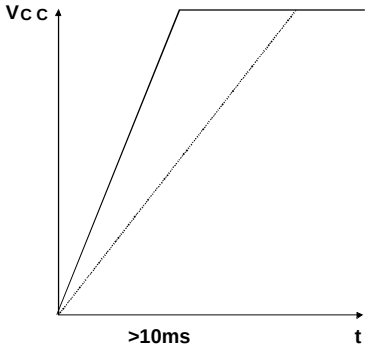


Fig 23 : Rise time power supply

The nominal supply voltage is 8V. With min/max values of 7.2- 8.8V. The total current consumption is 120mA, and about 60mA for each pin.
In stand-by condition the 8V IC-supply can be switched off as to save energy. After switching on the 8V again the normal start-up procedure must be followed.

A voltage detection circuit is connected to both pins.
Power-up: if the 8V increases >6.4V than; (after IC-initialisation and auto re-calibration)
H_D or **CLP** is released.

Power down: if the 8V drops <6.4V than; a power on reset, **POR**, is generated.
H_D or **CLP** is muted.
IC must be re-initialised.

Short supply decoupling is important for a stable horizontal drive.
Each supply pin supplies following internal circuit blocks:

pin11	**pin 45**
H/V sync	Chroma
Vision IF	Digital supply
Sound IF	
Filters	
Switches	

*** Digital supply decoupling,** **pin 33**

This decoupling pin is for the digital circuits. The recommended capacitor is 100nF. The pin voltage is 5V.
A power on reset, POR, is generated when V_{33} <4V

*** Bandgap decoupling,** **pin 35**

The bandgap circuit provides a very stable and temperature independent reference voltage and is used in all functional IC-circuit blocks.
This reference voltage is 4V. Optimal decoupling is achieved with two capacitors in parallel:
- low frequent decoupling (for stable H-drive): C=2µ2F
- high frequent decoupling: C=22nF

Short decoupling and separate ground track to pin 44 is advised.
For a correct calibration of the horizontal oscillator after power on the bandgap voltage must be stabilised.
During start-up the bandgap capacitor is pre-charged with 1mA during the first two vertical fields.
If C=2.2µF, than t= 6.7V*2.2µ/1mA= 15ms.
A power on reset, **POR**, is generated when V35<3.6V.

*** Grounding,** **pin 9, 31, 44**

For optimal performance its recommended to have both ground pins directly connected via a ground plane underneath the IC.

*** Pin protection for ESD** **all other pins**

All IC-pins have internal protection diodes, one to supply and one to ground for ESD protection, see Fig 24.
Under normal operation and supply-off condition these diodes may not conduct. Otherwise excessive current can flow through these diodes and/or internal circuit parts and the IC will be damaged.

All ESD protection diodes meet the specification of both Human body and Machine model.
Nevertheless for safe operation each pin voltage should remain in between:

- normal IC operation and supply is 8V: -0.7V …… +8.7V
- in stand-by condition and supply is 0V: -0.7V …… +0.7V

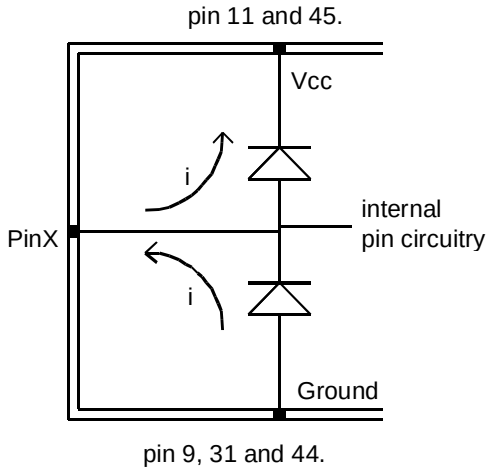


Fig 24 : ESD pin protection

Note:
- When the supply =0V avoid that IC pins are supplied by e.g. the micro processor for OSD signals. We have had no problems so far when the a continuous diode current is less than 1mA.
- The tuner AGC output pin 62 may have a higher voltage, V11 < V_{cc} + 1V. This makes the application with the tuner more easy.
- Maximum voltage for Y/U/V and CVBS input pins is 5.5V. This to avoid parasitic effects at the pin.

3.3 Application of non-used pins

Below a list is given of how to applicate non used pins.

# pin	**Description**	**Application if pin is not used**
Vision and Sound IF		
1	SIF-AGC	open and **IFO**=1
2, 3	VIF-inputs	open, connected together and/or grounded
4	VIF-AGC	open and **IFO**=1
5	QSS/AM output	open
6	PLL loopfilter	open
7, 8	VCO coil	open, connected together and/or grounded
10	Video output	open and **VSW**=1 and **IFO**=1
12	groupdelay in	C=10nF to ground
13	groupdelay out	open
19, 22	switched outputs	open and **OS0, OS1**=0
62	Tuner AGC output	open or grounded
63, 64	SIF-inputs	open, connected together and/or grounded
Filters an Switches		
16, 18, 20, 23, 28	CVBS and Yinputs	C=22nF to ground
21, 24, 29	Chroma inputs	to ground (don't leave open as to avoid pick-up due to high impedance)
26, 32, 34	CVBS outputs	open
15, 17	AV inputs	to ground
36, 37, 38, 41, 42, 43	RGB inputs	C=22nF to ground
39, 40	RGB insertion pins	to ground
Colour decoder		
54, 55, 56, 57	Xtal pins	open, always at least one Xtal applicated
30	Subcarrier ref. output	open
25, 27	COMBSYS outputs	open

4. ALIGNMENTS

4.1 IF-VCO

This alignment can be realised fully automatically by means of the I2C bus. This is a big advantage while having a fixed external VCO-coil. The tuning range is 3.7MHz with 128 steps, thus 29kHz/step typical. This 29kHz step is sufficient for PLL-tuners where frequency steps have to be <62.5kHz.

Procedure to be carried out in the TV production line:

- Have a fixed VCO-coil mounted according the specifications given
- Apply a 38.9MHz signal (or other standard frequency) to the IF-input
- Preset the VCO adjust, bits A0-A6 to 63 (middle of range). Set **L'FA** (A7) to 0.
- Align the VCO by means of VCO adjust bits A0-A6 for correct AFC information.
  The VCO adjustment is correct when the **AFA** bit is "1" and the **AFB** bit is altering.
  (this can be realised fully automatically by software)
- Store this VCO adjust setting into the non-volatile memory of the micro.

Remark: For SECAM L' (Set **L'FA** (A7) to 1) this procedure must be done twice; once for 38.9MHz and secondly for 33.4 or 33.9MHz. This is important because the frequency step of -5 or -5.5MHz are typical values only.

Therefore two VCO-adjust settings for both **L'FA**=0 and 1 must be loaded into the non-volatile memory of the micro. One of the VCO-adjust settings then can be recalled during channel switching, depending upon the TV-standard that is received.

4.2 Tuner AGC

With the I²C bus function the tuner take over point can be adjusted in 63 steps.

Apply a (e.g. 1mV) RF signal to the aerial input of the tuner. Increase by I²C bus the take over setting such that the voltage at the tuner output pin 62 drops 1V below its maximum voltage.

Notice:

- This adjustment requires a compromise between S/N ratio and intermodulation. The intermodulation will increase when the tuner output amplitude becomes too high. See tuner specification, often < 107dBµV.
- The IF-amplitude variation (slip) depends on the tuner AGC loop gain, see tuner output pin 62.
- The 1mV also depends on tuner gain and SAW filter insertion losses, see Fig 25 below.

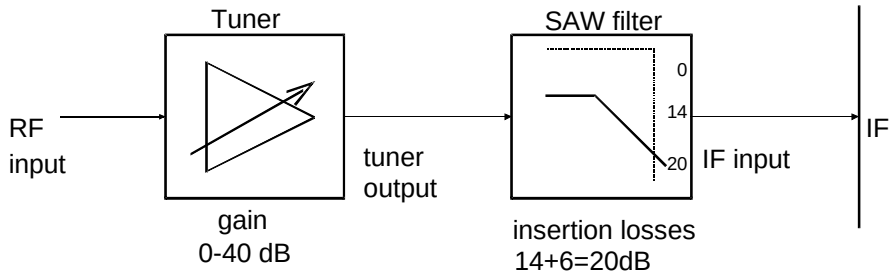


Fig 25 : RF to IF signal path.

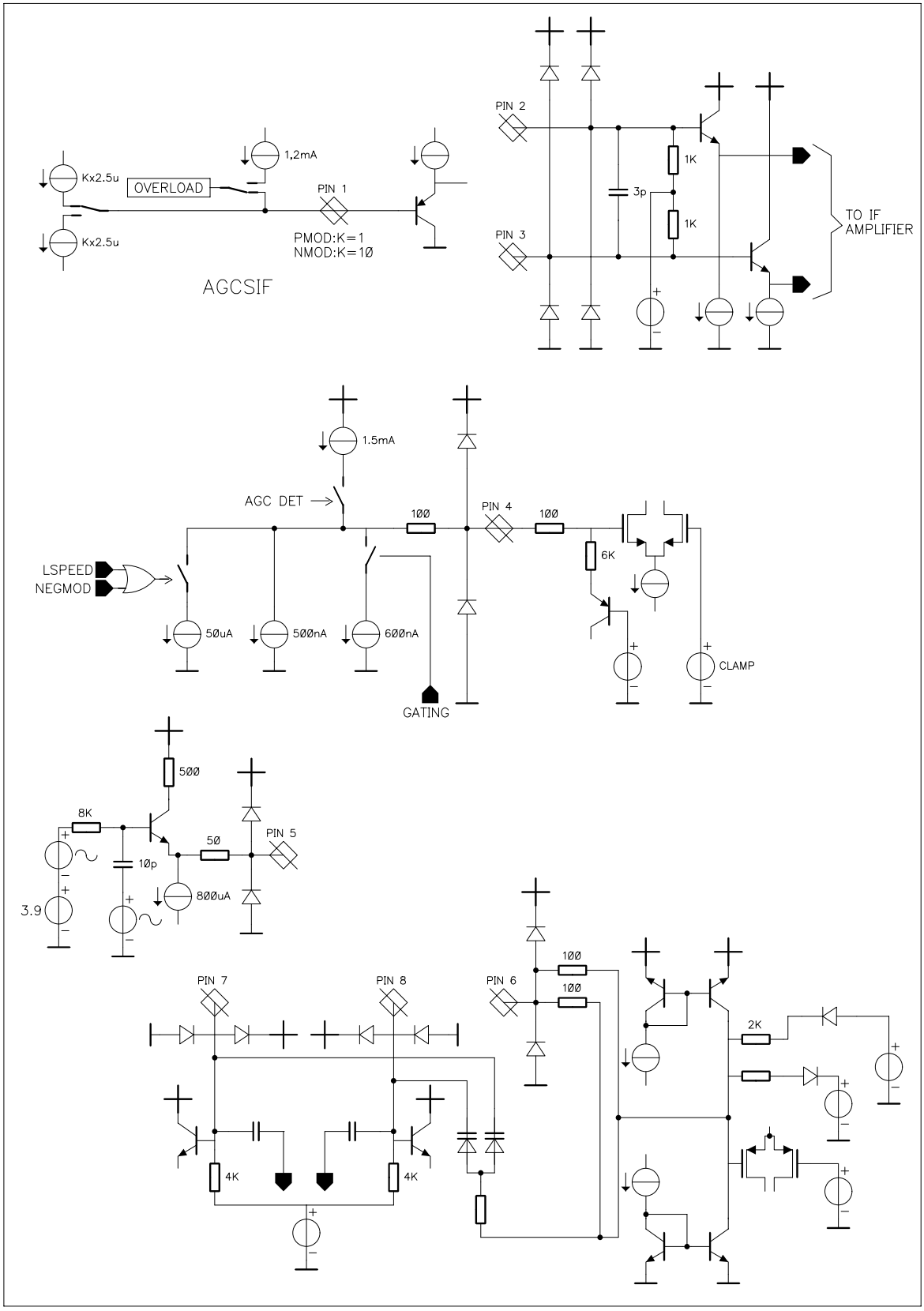
RF input	Tuner gain	Tuner output	SAW	IF input
1 mV	+40 dB	100 mV	-20 dB	10 mV
60 dBµV	+40 dB	100 dBµV	-20 dB	80 dBµV

Table 14 : RF to IF signal level.

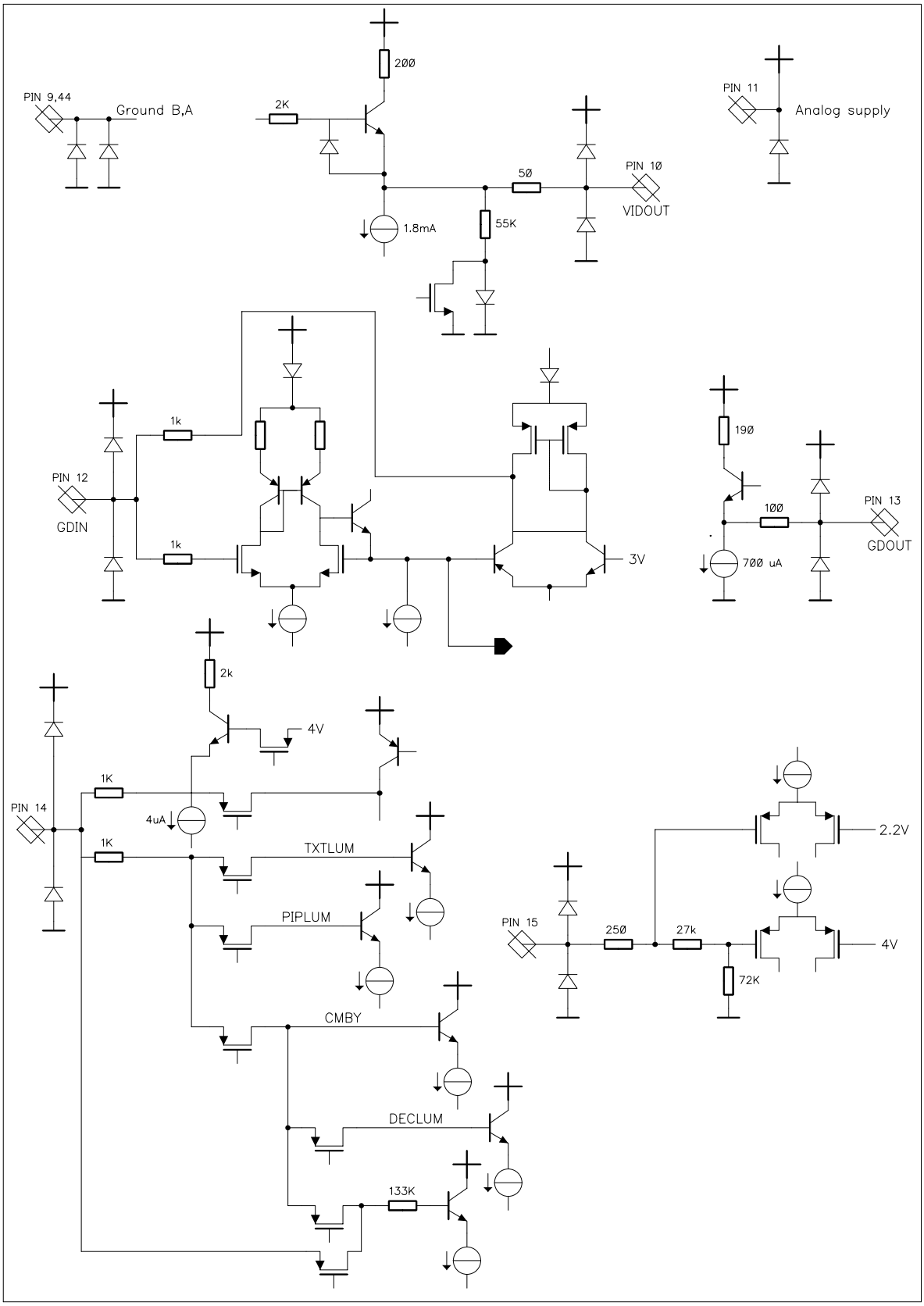
5. REFERENCES

1 Device specification, May 1998
TDA9320H, I2C-bus controlled TV input processor

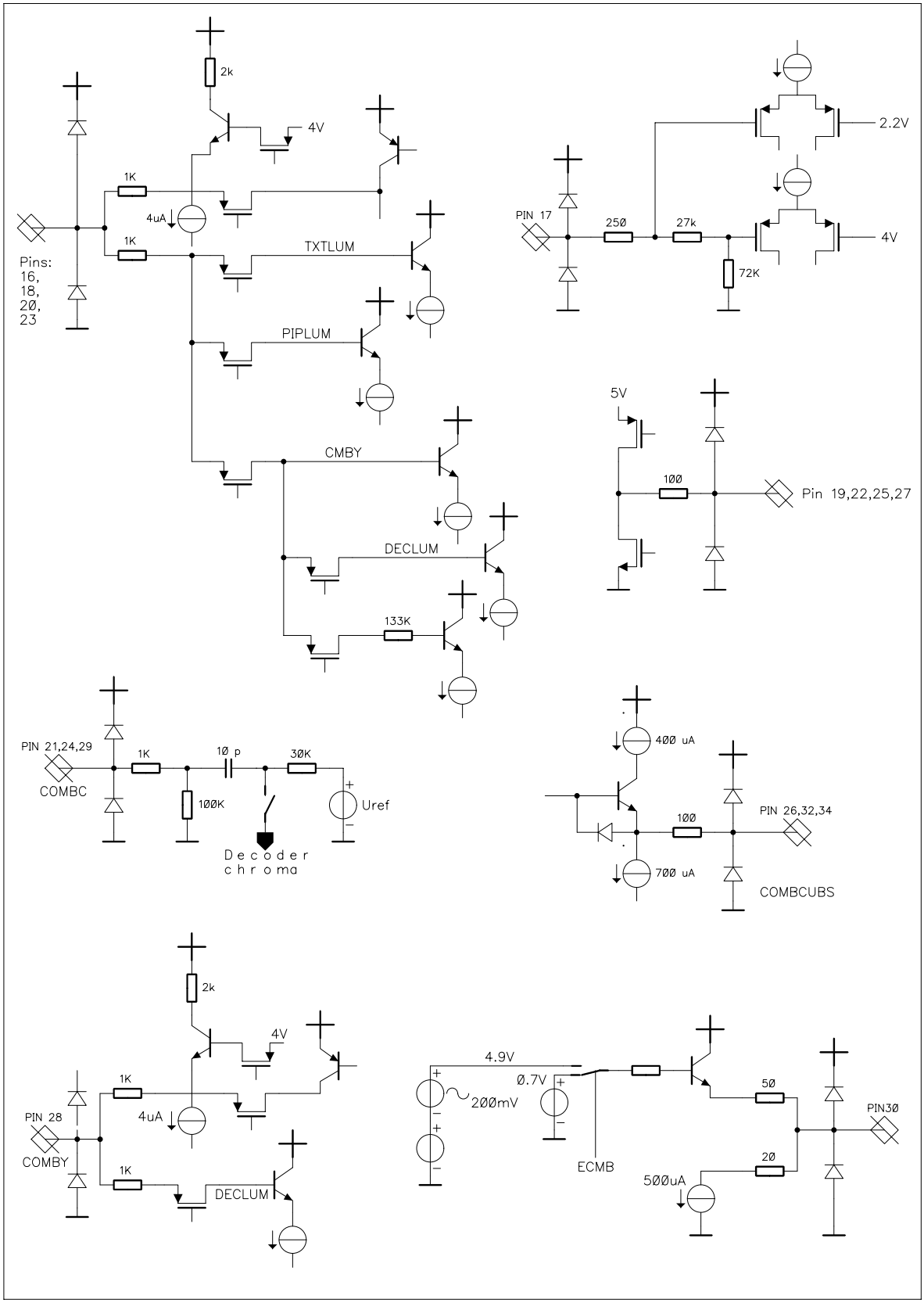
2 Application note AN98073, September 1998
TDA933X H, I2C-bus controlled TV display processor



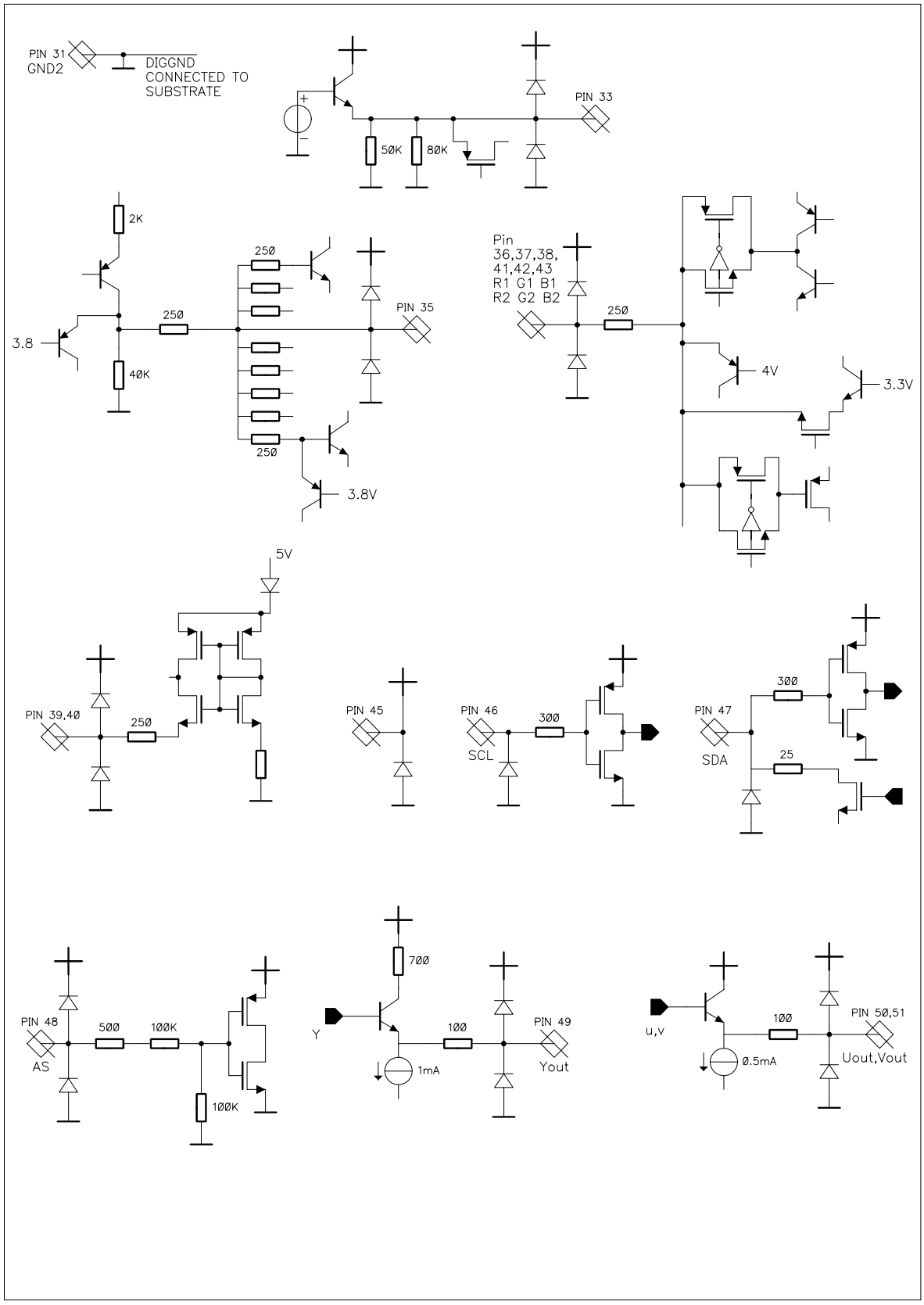
B 1 : Internal pin configuration (1-8)



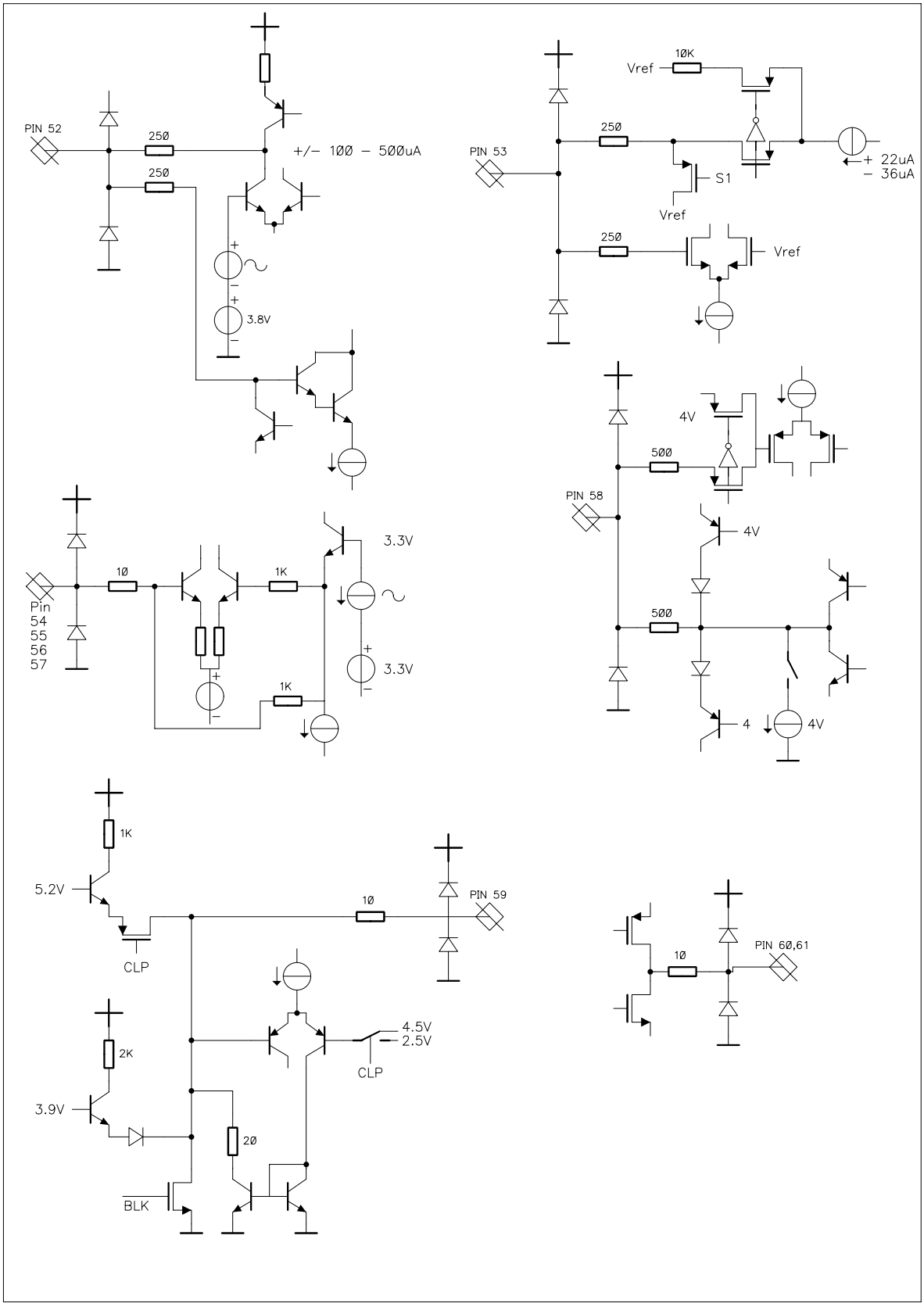
B 2 : Internal pin configuration (9-15)



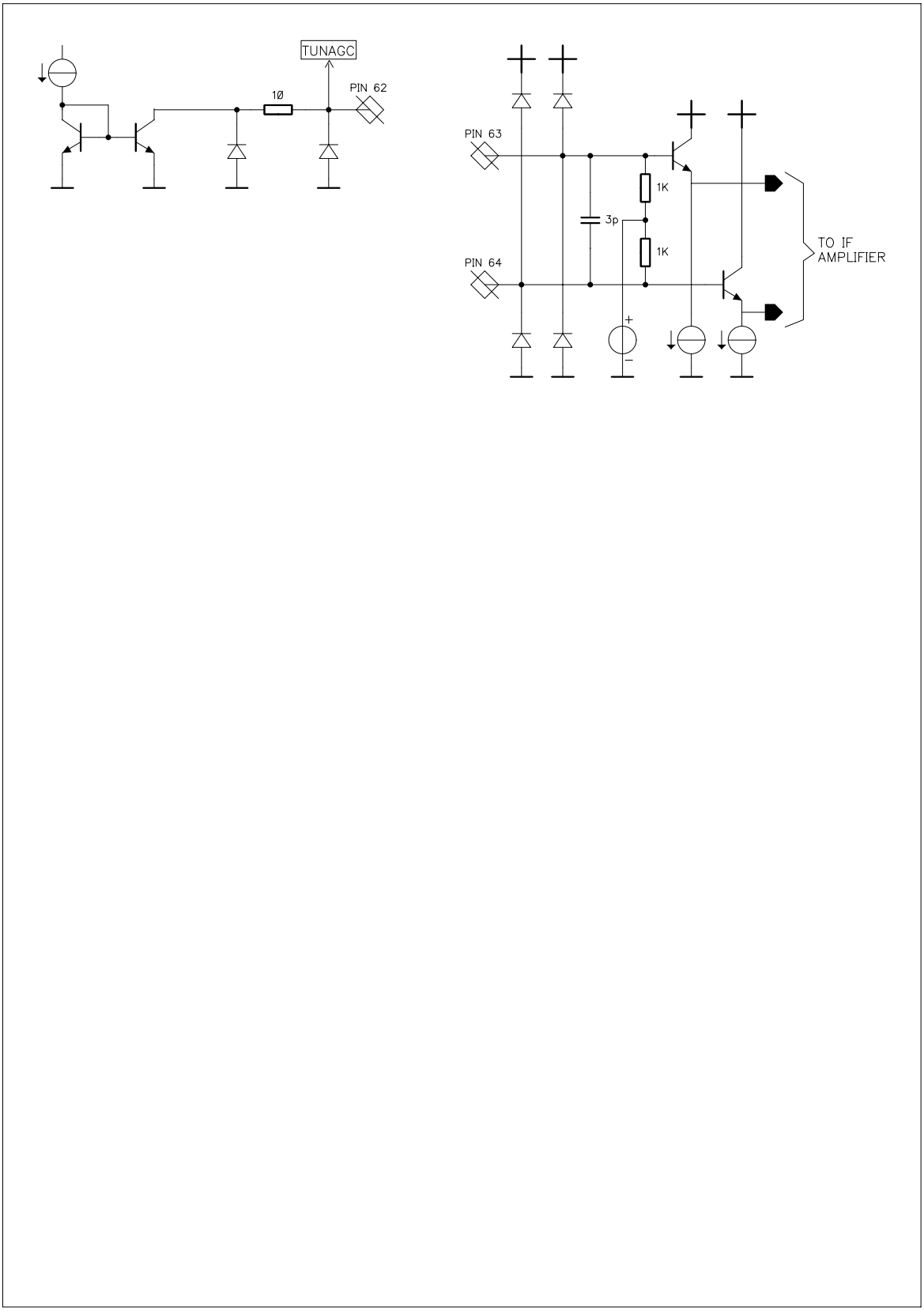
B 3 : Internal pin configuration (16-30)



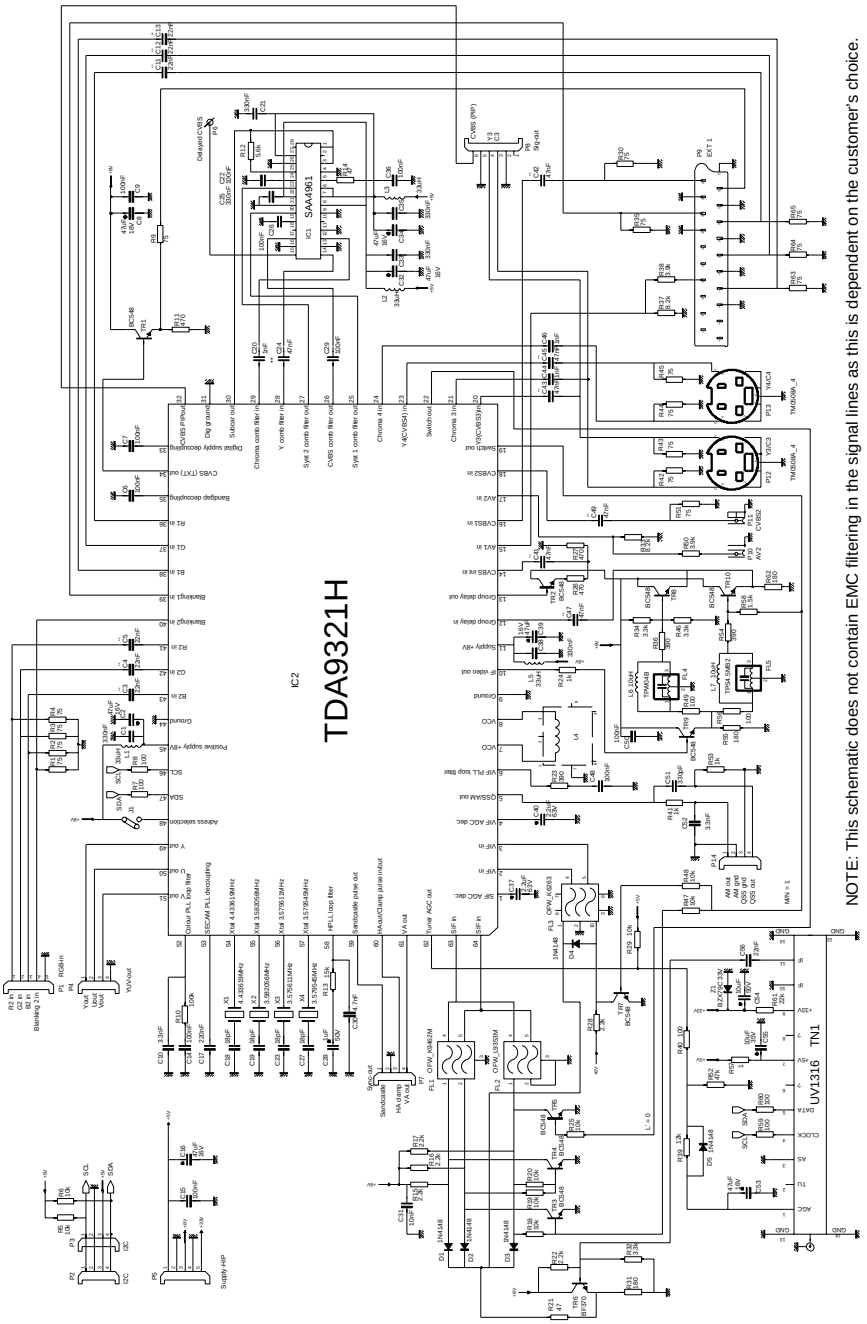
B 4 : Internal pin configuration (31-51)



B 5 : Internal pin configuration (52-61)



B 6 : Internal pin configuration (62-64)



C 1 : Application diagram for TDA9321 H

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
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Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
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